ANALYSIS AND CONTROL OF THE SYNCHRONOUS BUCK CONVERTER WITH A CONSTANT POWER LOAD

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This thesis examines the effects of loads with constant power characteristics on the operation of the synchronous buck converter. Loads with constant power characteristics occur when a regulated converter is used as a load, which is the case in power distribution architectures composed of power electronics converters rather than direct connection of sources, loads, or energy storage.

In this thesis, the large signal behavior and control of a system comprised of an ideal synchronous buck converter feeding an ideal constant power load are examined. A polar coordinate model of the system is derived for use in the analysis of both the constant duty cycle and controlled duty cycle behavior of the system, and the unstable nature of the single equilibrium point and the global absence of convergence to any point or limit cycle for non-equilibrium initial conditions is proven mathematically for the constant duty cycle case.

To stabilize the system, geometrical boundary control and PD control are examined. The analysis and design of the boundary controller in the polar coordinate representation is presented, and the region of convergence and local stabilization of the system under boundary control are verified using numerical simulation. The analysis and design of the PD controller is then presented using both small-signal techniques and geometrical insights from boundary control, and the region of convergence and local stabilization are verified using numerical simulation. Lastly, the addition of an integral component to the PD controller to compensate

for operating point changes, control signal error, and parameter uncertainty is analyzed using small-signal techniques, and performance of the system under PID control is verified using numerical simulation.

Throughout, simulation results from a switching model of a synchronous buck converter feeding a point of load buck converter are included to verify the performance of the control strategies in a more realistic circuit.

TABLE OF CONTENTS

PREFACE x

1.0 INTRODUCTION 1

2.0 POLAR COORDINATE ANALYSIS OF CPL BUCK CONVERTERS 5

2.1 CONSTANT DUTY CYCLE OPERATION WITH CPL 5

2.2 CONSTANT DUTY CYCLE SIMULATIONS 7

2.3 CONTROLLED DUTY CYCLE OPERATION WITH CPL 9

3.0 BOUNDARY CONTROL OF CPL BUCK CONVERTERS 12

3.1 INTRODUCTION TO BOUNDARY CONTROL 12

3.2 POLAR COORDINATE ANALYSIS OF BOUNDARY CONTROL 13

3.3 SIMULATION RESULTS WITH BOUNDARY CONTROL 19

4.0 PROPORTIONAL DERIVATIVE CONTROL OF CPL BUCK CONVERTERS 25

4.1 INTRODUCTION TO PROPORTIONAL DERIVATIVE CONTROL . . . 25

4.2 SMALL-SIGNAL STABILITY ANALYSIS OF PD COMPENSATED CPL BUCK CONVERTER 26

4.3 GEOMETRICAL AND LARGE-SIGNAL ANALYSIS OF PD COMPENSATED CPL BUCK CONVERTER 28

4.4 SIMULATION RESULTS WITH PD CONTROL 31

5.0 PROPORTIONAL INTEGRAL DERIVATIVE CONTROL OF CPL BUCK CONVERTERS FOR VOLTAGE REGULATION 36

5.1 SMALL-SIGNAL STABILITY ANALYSIS OF PID COMPENSATED CPL BUCK CONVERTER 37

5.2 SIMULATION RESULTS WITH PID CONTROL 38
6.0 CONCLUSIONS 43
APPENDIX A. DERIVATIONS 46
A.1 CONSTANT DUTY CYCLE POLAR COORDINATE DERIVATION . . . 46
A.2 CONTROLLED DUTY CYCLE POLAR COORDINATE DERIVATION . 47
A.3 LOAD CURVE POLAR COORDINATE DERIVATION 48
APPENDIX B. MODEL DETAILS 49
B.1 BOUNDARY CONTROL MODEL 50
B.2 PD CONTROL MODEL 51
B.3 PID CONTROL MODEL WITH DISTURBANCES 52
B.4 COMPONENT MODEL OF SYSTEM WITH CASCADED LRC AND POL CONVERTERS 53
BIBLIOGRAPHY 54

LIST OF TABLES

3.1 Test points for boundary point classification 16
3.2 Test points for reflective boundary point stability 18

LIST OF FIGURES

1.1 Synchronous Buck Converter Feeding a Regulated POL Converter 3

1.2 Synchronous Buck Converter Feeding an Ideal CPL 3

2.1 Constant Duty Cycle Simulation of Mathematical Model of Ideal CPL Synchronous Buck Converter 8

2.2 Constant Duty Cycle Simulation of Switching Model of Cascaded Converter System 9

3.1 Boundary Point Classification Illustration 14

3.2 Potential Transition Points For Boundary Point Classification 16

3.3 Boundary Point Classification Regions 17

3.4 Boundary Point Classification Regions With Reflective Point Stability 18

3.5 Boundary Control Separatrix Plot for $\theta_b = 115°$ 20

3.6 Boundary Control Separatrix Plots for for $\theta_b = 110°$, $116°$, $120°$ and $130°$ . . 21

3.7 Boundary Control Simulation State Space Trajectory Plots for $\theta_b = 116°$ . . . 22

3.8 Boundary Control Simulation Voltage and Current Waveforms for $\theta_b = 116°$. 23

3.9 Simulation of Switching Model of Boundary Controlled Cascaded Converter System 24

4.1 Block diagram for PD compensated converter 27

4.2 PD Duty Cycle Plots for $R_1 = 1$; $R_2 = 0.085$ and $R_1 = 1$; $R_2 = 0.2$ 30

4.3 PD Duty Cycle Plots for $R_1 = 0.2442$; $R_2 = \infty$ and $R_1 = 1$; $R_2 = \infty$ 30

4.4 PD Separatrix Plots for $R_1 = 1$; $R_2 = 0.085$, $R_1 = 1$; $R_2 = 0.2$, and $R_1 = 0.2442$; $R_2 = \infty$ 32

4.5 PD Separatrix Plots for $R_1 = 1$; $R_2 = \infty$ and $R_1 = 10$; $R_2 = \infty$ 33

4.6 PD State Space Trajectory and Waveforms for $R_1 = 1$; $R_2 = \infty$ and $R_1 = 10$; $R_2 = \infty$ 34
4.7 Simulation of Switching Model of PD Controlled Cascaded Converter System 35
5.1 Disturbance Plots With No Integral Control 39
5.2 Disturbance Plots With Integral Control 40
5.3 Simulation of Switching Model of PID Controlled Cascaded Converter System 41
B1 Mathematical Simulink Model of Boundary Controlled Synchronous Buck Converter with CPL 50
B2 Mathematical Simulink Model of PD Controlled Synchronous Buck Converter with CPL 51
B3 Mathematical Simulink Model of PID Controlled Synchronous Buck Converter with CPL and Disturbances 52
B4 SimPowerSystems Component Model of LRC and POL Converter System . . 53

PREFACE

ACKNOWLEDGMENTS

I would like to thank my advisor, Professor Alexis Kwasinski for his guidance with this thesis and my other research pursuits. I am grateful for his encouragement to pursue a loose thread that appeared in my attempts to model a DC microgrid system due to my choice to use synchronous converters rather than more standard asynchronous converters. That thread became this thesis, and the journey these past several months has been both interesting and rewarding.

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I would like to express my deep gratitude to my wife Erin for putting up with me throughout grad school while herself being seemingly buried alive in medical school. Her love and patient support so far in our marriage has meant the world to me, and I pray I can return the same to her for the rest of our lives.

Lastly, I would be woefully remiss if I didn't acknowledge the surpassing dependence the writing of this thesis has on the providence God. "For who has known the mind of the Lord, or who has been his counselor? Or who has given a gift to him that he might be repaid? For from him and through him and to him are all things. To him be glory forever. Amen" (Romans 11:34-36, ESV)

1.0 INTRODUCTION

This thesis examines the effects of constant power loads (CPLs) on the operation of the synchronous buck converter. Loads with constant power (CP) characteristics occur when a tightly regulated converter is used as a load, which is the case in power distribution architectures composed of power electronics converters rather than direct connection of sources, loads, or energy storage [1]. While power electronic power distribution architectures like this are widely used within specific loads such as computers, increasingly power distribution architectures composed of power electronics are being considered or implemented for cars, ships, airplanes, and facilities to take advantage of alternative energy sources or attempt to increase efficiency and system availability [2].

Because regulated point of load (POL) converters present CP behavior at their input terminals, the behavior of any source converter feeding a regulated POL converter cannot be assumed to be the same as if the load was resistive. For this reason, the control of dc-dc converters such as buck converters with CPL has long been a topic of research [1, 3–6]. A sampling of the literature reveals varied techniques have been proposed for the design of controls for the asynchronous buck converter with CPL, including linearized small-signal design of proportional integral derivative (PID) controls [3], nonlinear feadback linearization techniques [1], nonlinear large-signal analysis of PID controls [4], nonlinear passivity based control (PBC) derivation of proportional derivative (PD) controls [5], and geometrical boundary control [6]. Some of the approaches, such as that found in [4], consider a CPL in parallel with a resistive load which reduces the severity of the CP characteristics, but is often not a feasible mitigation strategy in power distribution architectures [5].

While the asynchronous buck converter studied in the previous CPL research discussed in the preceding paragraph switches using one transistor and one diode, the synchronous buck

converter replaces the diode with a transistor to switch with two active switches. Various motivations such as attempting to improve efficiency in lower duty cycle operation or reduce the converter size could lead to the choice to use a synchronous buck converter [7]. However, the discontinuous conduction mode (DCM) intrinsic to the asynchronous buck converter does not occur in the synchronous buck converter unless forced by control action [8], and the region of convergence observed in numerical analysis, simulation, and experimental results for the asynchronous buck converter cannot be assumed for the synchronous configuration. The reason for this is that the asynchronous configuration can rely on the stable limit cycle induced by DCM operation for low inductor currents near $i_L = 0$ to bring any trajectory that begins at $v_C > \overline{v_C}$ and approximately $i_L = 0$ to approximately $v_C = \overline{v_C}$; $i_L = 0$. As long as the control region of convergence includes $v_C = \overline{v_C}$; $i_L = 0$, therefore, the observed region of convergence for the asynchronous converter includes all trajectories that approach $i_L = 0$ at $v_C > \overline{v_C}$. Controls designed for the asynchronous buck converter with CPL are able to take advantage of the DCM and may not perform as desired in a synchronous buck converter. In this thesis, the PBC designed PD controls proposed in [5] and the boundary controls proposed in [6], both previously applied to the asynchronous buck converter, are examined for the synchronous buck converter.

Figure 1.1 shows a circuit schematic of the motivating example for this thesis, a synchronous buck converter used as a line regulating converter (LRC) feeding a regulated point of load (POL) converter that will present CP characteristics to the LRC.

The cascaded converter system in Figure 1.1 is well suited for circuit model simulation using tools like the SimPowerSystems libraries and analysis tools for MATLAB Simulink. For modeling and simulation in this thesis, circuit parameters $L_{LRC} = 500\mu H$, $C_{LRC} = 470\mu F$, $L_{POL} = 300\mu H$, $C_{POL} = 1.5mF$, $R = 0.72\Omega$, $K_{p;POL} = 5$, $K_{i;POL} = 10$, $E = 21.1V$, $V_{o;LRC} = 14V$, and $P_L = 45W$ will be used based on the converters studied in [5] to better enable comparison with the results for the PD-compensated asynchronous buck converter with CPL referenced. However, these parameters are close to those studied in [6] and the resulting simulation results should allow for comparison with the referenced results for the boundary controlled asynchronous buck converter with CPL.

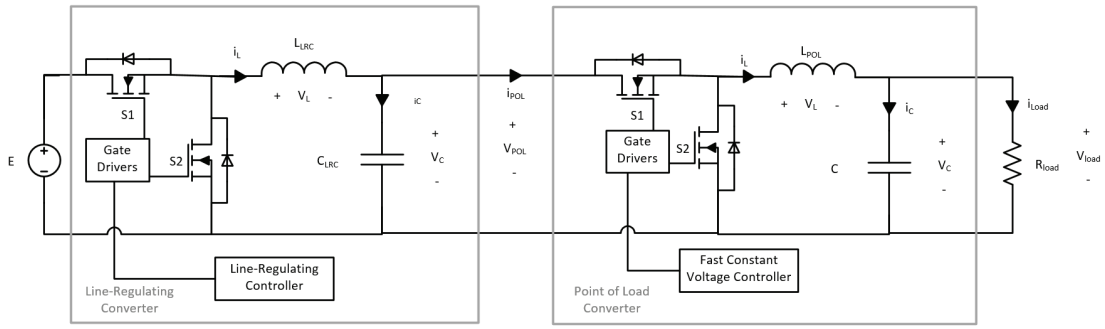


Figure 1.1: Synchronous Buck Converter Feeding a Regulated POL Converter

To examine a CPL that demonstrates CP behavior for all nonzero voltages, the POL converter can be replaced with an ideal CPL as shown in Figure 1.2 for analysis of the converter and proposed controllers. The ideal CPL synchronous buck converter system shown in Figure 1.2 will be the focus of mathematical analysis, modeling, and simulation in this thesis, with the cascaded converter system of Figure 1.1 being used for performance verification in a more realistic circuit.

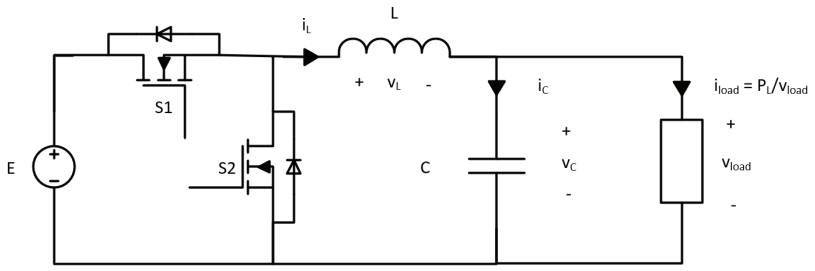


Figure 1.2: Synchronous Buck Converter Feeding an Ideal CPL

The rest of this thesis is organized as follows. Chapter 2 presents mathematical analysis of the system shown in Figure 1.2, including the derivation of a polar coordinate representation

which gives additional insight into stability and convergence issues with the CPL converter. Simulation results demonstrating the stability and convergence issues in both the ideal CPL system and cascaded converter system are also included in Chapter 2. Chapter 3 examines boundary control for controlling the ideal CPL system and verifies through simulation the performance with the POL system. Similarly, Chapter 4 examines PD control for controlling the ideal CPL system and verifies the performance through simulation. Chapter 5 examines the introduction of an integral controller action to the PD control to compensate for operating point changes, control error, parameter uncertainty, and circuit losses. Chapter 6 provides conclusions and ends the body of the thesis, while derivation details and figures of the models used for simulation are left for the appendices.

2.0 POLAR COORDINATE ANALYSIS OF CPL BUCK CONVERTERS

Before addressing control of the synchronous buck converter with a CPL, a polar coordinate representation for the buck converter is derived to provide additional insight into the stability and convergence issues with the CPL buck converter.

2.1 CONSTANT DUTY CYCLE OPERATION WITH CPL

To examine the impact of an ideal CPL on the synchronous buck converter, the constant duty cycle case is first examined. With constant duty cycle D, the equations defining the fast-averaged model of the ideal CPL synchronous buck converter from Figure 1.2 are given in (2.1).

$$\begin{aligned} \frac{dv_C}{dt} &= \frac{1}{C}\left(i_L - \frac{P_L}{v_C}\right) \\ \frac{di_L}{dt} &= \frac{1}{L}\left(DE - v_C\right) \end{aligned} \tag{2.1}$$

The equilibrium voltage and current are found by setting both derivatives to zero and solving for v_C and i_L, yielding $\overline{v_C} = DE$ and $\overline{i_L} = \frac{P_L}{\overline{v_C}} = \frac{P_L}{DE}$. To better understand the behavior in relation to this equilibrium point, a coordinate change is introduced as defined in (2.2). The duty cycle displacement variable is also defined in (2.2), but is zero for the constant duty cycle case.

$$\begin{aligned} \widetilde{v_C} &:= v_C - \overline{v_C} \\ \widetilde{i_L} &:= i_L - \overline{i_L} \\ \widetilde{d} &:= d - D \end{aligned} \tag{2.2}$$

Using the change of coordinates, the first order differential equations for the new displacement variables are given in (2.3).

$$\begin{aligned}\frac{d\widetilde{v_C}}{dt} &= \frac{1}{C}\left(\widetilde{i_L} + \overline{i_L}\left(\frac{\widetilde{v_C}}{\widetilde{v_C} + \overline{v_C}}\right)\right) \\ \frac{d\widetilde{i_L}}{dt} &= -\frac{1}{L}\left(\widetilde{v_C}\right)\end{aligned} \tag{2.3}$$

From the differential equations, it can be verified that the equilibrium point exists. It can also be seen that a first derivative discontinuity exists at $\widetilde{v_C} = -\overline{v_C}$, characterized by differing left and right limits of the first derivative of $\widetilde{v_C}$ as shown in (2.4).

$$\begin{aligned}\lim_{\widetilde{v_C} \to -\overline{v_C}^-} \frac{d\widetilde{v_C}}{dt} &= \infty \\ \lim_{\widetilde{v_C} \to -\overline{v_C}^+} \frac{d\widetilde{v_C}}{dt} &= -\infty\end{aligned} \tag{2.4}$$

In fact, the infinite limits of the first derivative indicate that a singularity exists when the capacitor voltage reaches zero. This is because an ideal constant power load of nonzero power consumption cannot exist at zero voltage, since $P_{ld} = I_{ld}V_{ld} = I_{ld}(0V) = 0W$ regardless of the magnitude of the current.

It is clear from the differential equations in (2.3) that the system must avoid reaching this singularity to maintain operation, but it is not immediately clear from the equations whether the equilibrium point for the constant duty cycle case is locally stable. To provide some new intuition into the operation of this system, a transformation of the rectangular coordinate representation of the system to an energy based polar coordinate representation is introduced. First, a change of variables is defined in 2.5.

$$\begin{aligned} r &:= \sqrt{\frac{C}{2}\left(\widetilde{v_C}^2\right) + \frac{L}{2}\left(\widetilde{i_L}^2\right)} \\ \theta &:= \begin{cases} \tan^{-1}\left(\sqrt{\frac{L}{C}}\left(\frac{\widetilde{i_L}}{\widetilde{v_C}}\right)\right) & \widetilde{v_C} \geq 0 \\ \tan^{-1}\left(\sqrt{\frac{L}{C}}\left(\frac{\widetilde{i_L}}{\widetilde{v_C}}\right)\right) + \pi & \widetilde{v_C} \leq 0 \end{cases} \end{aligned} \tag{2.5}$$

Next, the first derivatives for this new representation are calculated. For this, the identities for $\widetilde{v_C}$ and $\widetilde{i_L}$ in terms of the new variables are needed. Note that r in (2.5) is by definition nonnegative.

$$\begin{aligned} \widetilde{v_C} &= \sqrt{\frac{2}{C}}\left(r\cos\left(\theta\right)\right) \\ \widetilde{i_L} &= \sqrt{\frac{2}{L}}\left(r\sin\left(\theta\right)\right) \end{aligned} \tag{2.6}$$

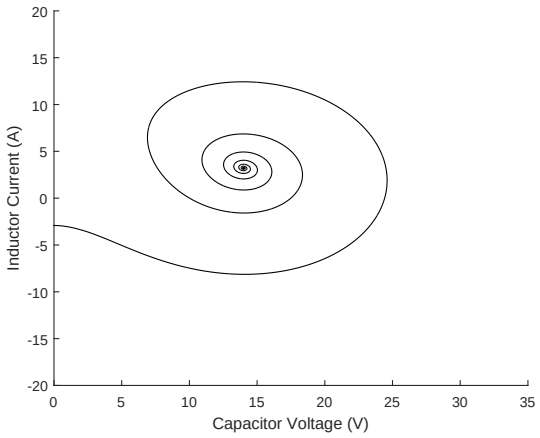
From these identities, the system of differential equations for the polar representation of the constant power load buck converter with constant duty cycle is derived in Appendix A in (A.1)-(A.10). Taking the first order differential equation results from (A.3) and (A.10), the polar representation is given by 2.7.

$$\begin{aligned} \frac{dr}{dt} &= \frac{\overline{i_L} r\cos^2\theta}{C\left(\sqrt{\frac{2}{C}}r\cos\theta + \overline{v_C}\right)} \\ \frac{d\theta}{dt} &= \frac{-1}{\sqrt{LC}} - \frac{\overline{i_L}\sin\theta\cos\theta}{C\left(\sqrt{\frac{2}{C}}r\cos\theta + \overline{v_C}\right)} \end{aligned} \tag{2.7}$$

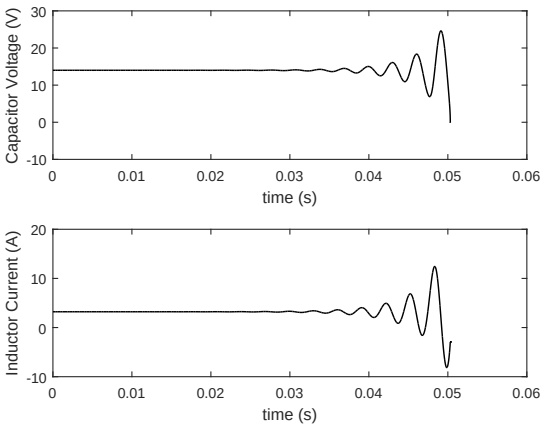
From $\frac{dr}{dt}$ in (2.7), it is clear that the system equilibrium point is locally unstable and that the system as a whole will not converge to any point or limit cycle, since $\frac{dr}{dt} \geq 0$ for all positive capacitor voltages.

2.2 CONSTANT DUTY CYCLE SIMULATIONS

To demonstrate the divergence of the ideal CPL synchronous buck converter system shown in Figure 1.2 and modeled mathematically using the fast-averaged converter equations, numerical simulation results from a model of (2.1) in MATLAB Simulink are shown in Figure 2.1. The initial conditions for the simulation are the equilibrium current and $0.1mV$ from the equilibrium voltage. The results in Figure 2.1 show that the system trajectory spirals out from the equilibrium point until it reaches $v_C = 0V$ and illustrates the orbital behavior that motivated the selection of polar coordinates to analyze the system behavior.



(a) State Space System Trajectory



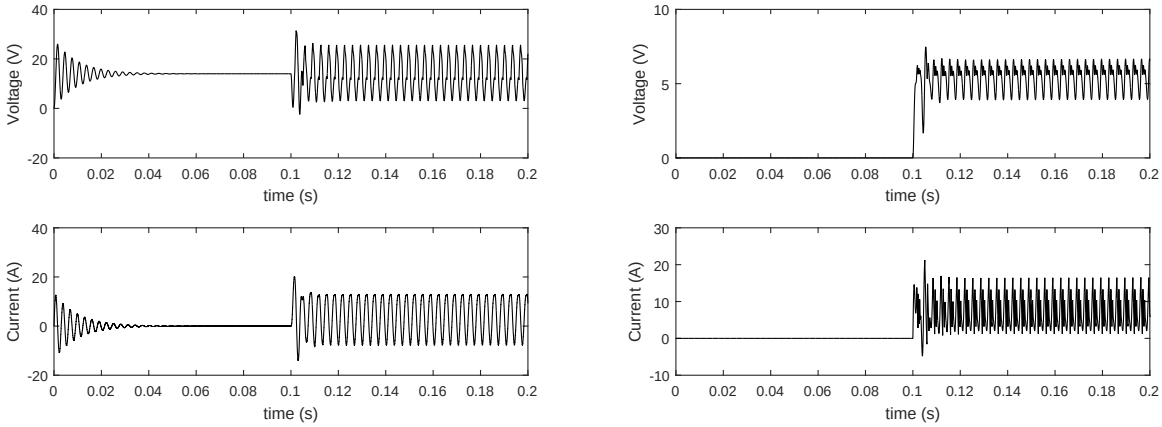
(b) Voltage and Current Waveforms

Figure 2.1: (a) State Space System Trajectory and (b) Voltage and Current Waveforms for Constant Duty Cycle Simulation of Mathematical Model of Ideal CPL Synchronous Buck Converter

To introduce the difficulties CP characteristics of a POL converter cause for a constant duty cycle LRC converter, simulation LRC voltage and current waveforms from a constant duty cycle SimPowerSystems simulation of the cascaded converter system shown in Figure 1.1 are presented in Figure 2.2. The SimPowerSystems switching model of the cascaded converter system developed and simulated for this thesis is included in Figure B4 in Appendix B. At $0.1s$ in the simulation, the voltage reference for the POL converter is increased from $0V$ to $5.83V$, corresponding to an attempted power increase from $0W$ to approximately $45W$.

Figure 2.2 (a) shows an initial transient as the buck converter reaches steady state with $0W$ output power before $0.1s$ and sustained LRC voltage and current oscillations after $0.1s$. Figure 2.2 (b) shows the simulation POL converter voltage and current waveforms, demonstrating that the POL converter is unable to regulate its capacitor voltage and load power due to the LRC output voltage oscillations. The inability of the POL converter to regulate

its load power indicates that it is in fact not presenting an ideal CPL to the LRC converter resulting in stable limit cycle behavior for the LRC rather than the divergence shown in Figure 2.1 for the ideal CPL buck converter model.



(a) LRC Waveforms

(b) POL Waveforms

Figure 2.2: (a) LRC and (b) POL Converter Voltage and Current Waveforms for Constant Duty Cycle Simulation of Switching Model of Cascaded Converter System

2.3 CONTROLLED DUTY CYCLE OPERATION WITH CPL

Given the lack of convergence to equilibrium in constant duty-cycle operation of the ideal CPL synchronous buck converter mathematically proven in Section 2.1 and demonstrated through simulation in Section 2.2, the constant duty cycle polar coordinate representation will now be extended to the case of a controlled duty cycle to provide insight into control

strategies and convergence of the system under control. The system defined in (2.1) is adapted for controlled duty cycle operation in (2.8) by substituting instantaneous duty cycle d for constant duty cycle D.

$$\begin{aligned} \frac{dv_C}{dt} &= \frac{1}{C}\left(i_L - \frac{P_L}{v_C}\right) \\ \frac{di_L}{dt} &= \frac{1}{L}\left(dE - v_C\right) \end{aligned} \tag{2.8}$$

For the constant duty-cycle case in Section 2.1, a change of coordinates was introduced in (2.2) to measure the displacement of the voltages and currents from the equilibrium point. With varying duty-cycle, however, the equilibrium point is no longer constant, and constant reference points for duty-cycle, voltage, and current should be chosen from the desired voltage operating point.

$$\begin{aligned} D &:= \frac{v_{OP}}{E} \\ \overline{v_C} &:= v_{OP} = DE \\ \overline{i_L} &:= \frac{P_L}{v_{OP}} = \frac{P_L}{DE} \end{aligned} \tag{2.9}$$

Using the reference points in (2.9), the coordinate change defined (2.2) can be applied to (2.8) as given in (2.10).

$$\begin{aligned} \frac{d\widetilde{v_C}}{dt} &= \frac{1}{C}\left(i_L - \frac{P_L}{v_C}\right) = \frac{1}{C}\left(\widetilde{i_L} + \overline{i_L}\left(\frac{\widetilde{v_C}}{\widetilde{v_C} + \overline{v_C}}\right)\right) \\ \frac{d\widetilde{i_L}}{dt} &= \frac{1}{L}\left(dE - v_C\right) = \frac{1}{L}\left(dE - \overline{v_C} - \widetilde{v_C}\right) \end{aligned} \tag{2.10}$$

From the first order differential equations in (2.10), the change to the energy based polar coordinate representation of the system can be performed using the definitions in (2.5)and (2.6). In this new representation, $\frac{dr}{dt}$ and $\frac{d\theta}{dt}$ must be derived again using the update to

$\frac{d\widetilde{i_L}}{dt}$ given in equation (2.10). This derivation is presented in Appendix A in (A.11)-(A.18). From this derivation, (2.11) gives the system of differential equations defining the polar representation for the constant power load buck converter with variable duty cycle.

$$\begin{aligned}\frac{dr}{dt} &= \frac{1}{2r}\frac{dr^2}{dt} = \frac{\overline{i_L} r\cos^2\theta}{C\left(\sqrt{\frac{2}{C}}r\cos\theta + \overline{v_C}\right)} + \frac{\sin\theta\,(dE - \overline{v_C})}{\sqrt{2L}} \\ \frac{d\theta}{dt} &= -\frac{1}{\sqrt{LC}} - \overline{i_L}\left(\frac{\sin\theta\cos\theta}{C\left(\sqrt{\frac{2}{C}}r\cos\theta + \overline{v_C}\right)}\right) + \frac{\cos\theta\,(dE - \overline{v_C})}{\sqrt{2L}r}\end{aligned} \tag{2.11}$$

Comparing the system given by (2.7) to the system given by (2.11), it can be seen that allowing the duty-cycle to be controlled adds an additional term to each differential equation. This new term means that $\frac{dr}{dt}$ in (2.11) is not strictly nonnegative, showing the mechanism by which the system may be stabilized by a controller. The polar representation of the system will be applied to the analysis of a boundary controller in Chapter 3.

3.0 BOUNDARY CONTROL OF CPL BUCK CONVERTERS

Boundary control is a type of state space geometrical control where state trajectories crossing a switching surface are used to provide the control condition for switching operations. Boundary control has been applied in [6] to give local stability of asynchronous buck converters with CPLs, but the application to synchronous converters was not there considered. In this chapter, Section 3.1 introduces boundary control for buck converters, boundary control is analyzed for the ideal CPL synchronous buck converter in Section 3.2 using the polar coordinate representation introduced in chapter 2, and simulation is used to verify the performance of boundary control of both the ideal CPL and cascaded converter system models in Section 3.3.

3.1 INTRODUCTION TO BOUNDARY CONTROL

The basic concepts and theories of boundary control for DC-DC converters are defined and analyzed in [9], and were later extended to constant power loading of buck converters in [6] and boost and buck-boost converters in [10]. The boundary definition for control of a buck converter from [6] is given in (3.1).

$$\lambda : i_L = k\left(v_C - \overline{v_C}\right) + \overline{i_L} \tag{3.1}$$

In Chapter 2, the analysis assumed the fast-averaged model of the converter and considered duty cycle variable d. However, with boundary control, the switching function $q(t)$, which takes binary values of 0 or 1, is directly controlled by the controller. Using the boundary in (3.1), $q = 1$, switch S_1 is on, and S_2 is off when the inductor current

$i_L < k\left(v_C - \overline{v_C}\right) + \overline{i_L}$, and $q = 0$, S_2 is on, and S_1 is off when $i_L > k\left(v_C - \overline{v_C}\right) + \overline{i_L}$. In this manner, the control of the switches is enacted based on measurements at the most recent sample time, and the controller is memoryless.

In Section 3.2, the analysis from [6] will be reviewed and adapted for the polar coordinate representation of the synchronous configuration studied in this thesis.

3.2 POLAR COORDINATE ANALYSIS OF BOUNDARY CONTROL

The first step in analyzing the boundary controller in the polar representation is to determine the equation for the boundary in the new coordinates. The equivalent boundary can be derived from (2.10) and (3.1) and is given in (3.2).

$$\lambda : \theta = \begin{cases} \tan^{-1}\left(k\sqrt{\frac{L}{C}}\right) & \widetilde{v_C} \geq 0 \\ \tan^{-1}\left(k\sqrt{\frac{L}{C}}\right) + \pi & \widetilde{v_C} \leq 0 \end{cases} \tag{3.2}$$

For simplicity, $\theta_b := \tan^{-1}\left(k\sqrt{\frac{L}{C}}\right) + \pi$ can be defined to place θ_b in the second or third quadrant ($\widetilde{v_C} \leq 0$). With this definition of the boundary, the converter is operated with $q = 1$, switch S_1 on, and S_2 off for $\theta_b < \theta < \theta_b + \pi$ (below the boundary) and $q = 0$, S_2 on, and S_1 off for $\theta_b + \pi < \theta < \theta_b$ (above the boundary). (Note that θ should be considered modulus 2π, such that $\theta_b + \pi = \theta_b - \pi$)

With the boundary defined, the next step in analyzing boundary control of a system is to determine system behavior at the boundary. The converter state space should be analyzed to classify the points making up the boundary based on system behavior at each point. As illustrated in Figure 3.1, points on a boundary can be refractive, reflective, or rejective, depending on the system trajectory directions on either side of the boundary [9]. For trajectory analysis at the boundary points for the buck converter, $\dot{\theta}_0$ and $\dot{r}_0$ are defined as the first derivatives of θ and r at a boundary point with $q = 0$, and $\dot{\theta}_1$ and $\dot{r}_1$ are defined as the first derivatives for $q = 1$. Refractive points are defined as having trajectories approaching the boundary from one side and moving away from the boundary on the other, meaning either $\dot{\theta}_0 < 0 \wedge \dot{\theta}_1 < 0$ or $\dot{\theta}_0 > 0 \wedge \dot{\theta}_1 > 0$. Reflective points are defined as having

trajectories approaching the boundary on both sides, meaning $\dot{\theta}_0 > 0 \wedge \dot{\theta}_1 < 0$ for $\theta = \theta_b$ or $\dot{\theta}_0 < 0 \wedge \dot{\theta}_1 > 0$ for $\theta = \theta_b + \pi$. Rejective points are defined as having trajectories moving away from the boundary on both sides, which means $\dot{\theta}_0 < 0 \wedge \dot{\theta}_1 > 0$ for $\theta = \theta_b$ or $\dot{\theta}_0 > 0 \wedge \dot{\theta}_1 < 0$ for $\theta = \theta_b + \pi$.

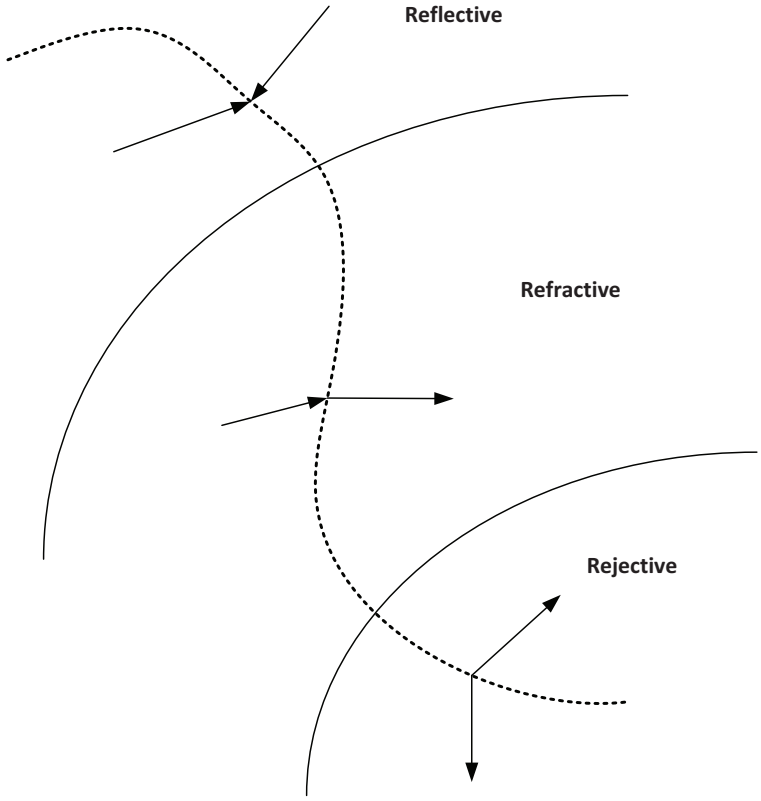


Figure 3.1: Boundary Point Classification Illustration

The transitions between boundary point classifications will occur at points in the system state space where either $\dot{\theta}_0 = 0$ or $\dot{\theta}_1 = 0$. Substituting switching function q for duty cycle d and solving for $\frac{d\theta}{dt} = 0$ in (2.11) results in the nonlinear quadratic equation in (3.3).

$$\begin{aligned}\left(\frac{-2\cos\theta}{C}\right) r^2 + \left(\sqrt{\frac{2}{C}}\left(-\overline{v_C} - \overline{i_L}\sqrt{\frac{L}{C}}\sin\theta\cos\theta + (qE - \overline{v_C})\cos^2\theta\right)\right) r \\ + \overline{v_C}(qE - \overline{v_C})\cos\theta \\ = a(\theta)r^2 + b(q,\theta)r + c(q,\theta) = 0\end{aligned} \tag{3.3}$$

(3.3) can be solved for r in terms of q and θ using the quadratic formula, giving closed form expressions for potential transition points in (3.4).

$$r(q,\theta) = \frac{-b(q,\theta) \pm \sqrt{(b(q,\theta))^2 - 4a(\theta)c(q,\theta)}}{2a(\theta)} \tag{3.4}$$

Using (3.4), the locus of potential transition point can be plotted in four parts in the state space as shown in Figure 3.2, with any imaginary roots of (3.3) eliminated. The four components of the locus are ϕ_{0p} and ϕ_{0m}, defined as the two curves given by the plus and minus results of $r(0,\theta)$ from (3.4), and ϕ_{1p} and ϕ_{1m}, the two curves given by the results of $r(1,\theta)$.

The locus of potential transition points divides the state space into four regions. To determine the boundary point classifications in each region, the signs of $\dot{\theta}_0$ and $\dot{\theta}_1$ in each region are determined using the test points shown in Table 3.1. Using the test points, the boundary point classification for each region is shown in Figure 3.3.

In order to determine stability of a boundary in a reflective mode region, it must be determined whether the system trajectories point towards or away from the desired operating point on the boundary. To do this, $\dot{r}$ can be examined with the assumption that $\dot{\theta} = 0$ since the boundary is defined by a constant value of θ. Since the system will be switching on the boundary at the maximum switching frequency allowed by the controller rather than leaving

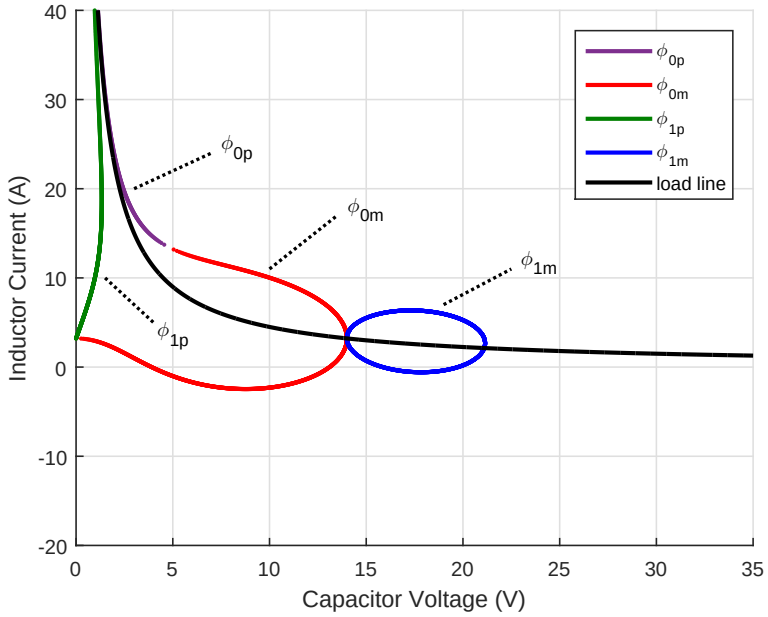


Figure 3.2: Potential Transition Points For Boundary Point Classification

Table 3.1: Test points for boundary point classification

v_C (V)	i_L (A)	$\dot{\theta}_0$ (rad/s)	$\dot{\theta}_1$ (rad/s)	Classification
1	0	-1614.5	-4758.2	Refractive
5	0	318.98	-3939.4	Reflective
16	3	-16282	5218.6	Reflective
0.5	20	5378.6	4159.5	Refractive

the boundary with either $q = 0$ or $q = 1$, $\frac{d\theta}{dt}$ from (2.11) is used to solve for the fast average duty cycle d that produces the assumption, $\dot{\theta} = 0$. The resulting equation for the duty cycle is given by (3.5).

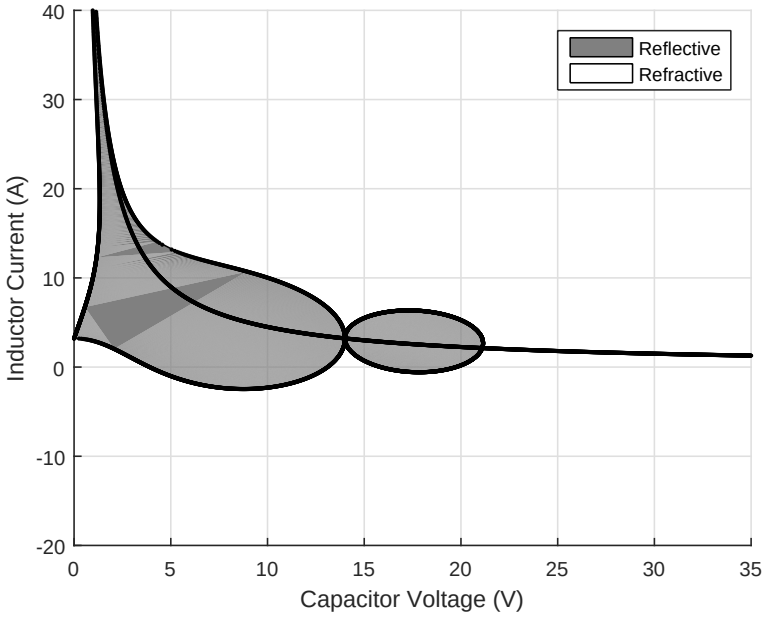


Figure 3.3: Boundary Point Classification Regions

$$d = \left(\frac{r\sqrt{\frac{2}{C}}}{E\cos\theta} \right) + \frac{\overline{i_L}}{E} \left(\frac{r\sqrt{2L}\sin\theta}{C\left(\sqrt{\frac{2}{C}}r\cos\theta + \overline{v_C}\right)} \right) + \frac{\overline{v_C}}{E} \tag{3.5}$$

Substituting (3.5) into $\frac{dr}{dt}$ from (2.11) yields two sets of values for r which result in $\dot{r} = 0$. The resulting equations are given in (3.6).

$$\begin{aligned} r_1 &= 0 \\ r_2 &= \frac{-\overline{v_C}\sqrt{\frac{C}{2}}}{\cos\theta} + \frac{-\overline{i_L}\sqrt{\frac{L}{2}}}{\sin\theta} \end{aligned} \tag{3.6}$$

Together, r_1 and r_2 from (3.6) are shown in Section A.3 of Appendix A to make up exactly the constant power curve $i_L = \frac{P_L}{v_C}$.

To classify the reflective mode regions as stable or unstable, test points can be selected in each of the four reflective mode regions as shown in Table 3.2. From these test points, the boundary point classification regions can be updated to show the stability of the reflective regions as seen in Figure 3.4.

Table 3.2: Test points for reflective boundary point stability

v_C (V)	i_L (A)	d	$\dot{r}$ $(J^{0.5}/s)$	Classification
10	0	0.2916	190.633	Unstable Reflective
10	9	0.1458	-263.609	Stable Reflective
20	1	0.9711	-43.624	Stable Reflective
20	4	0.9594	57.597	Unstable Reflective

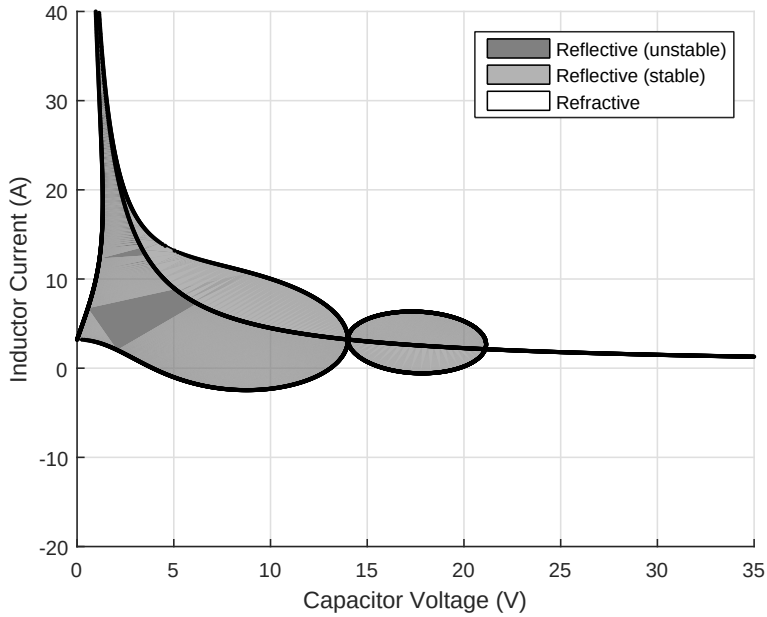


Figure 3.4: Boundary Point Classification Regions With Reflective Point Stability

With the state space divided into boundary point classification regions using the preceding analytical methods, the selection of a boundary should avoid the unstable reflective region, especially close to the desired operating point. From Figure 3.4, this indicates a negatively sloped boundary with $\pi/2 < \theta_b < \theta_{tan}$, where θ_{tan} designates the second quadrant tangent of the load line at the desired operating point. Choosing a boundary in this range,

it can be expected that if the converter operating point trajectory reaches the boundary in stable reflective region, the converter will be driven to the desired operating point, achieving stable operation. Boundary control stability in the refractive region is more difficult to analyze, requiring the analysis of the evolution of system trajectories between boundary intersections as shown in [9]. For this reason, the consideration of the stability in the refractive region will be left for demonstration through numerical simulation in Section 3.3.

3.3 SIMULATION RESULTS WITH BOUNDARY CONTROL

To demonstrate the region of convergence for boundary control of the ideal CPL system with boundary angle θ_b, the separatrix can be obtained from numerical simulation of the system differential equations from (2.8) in reverse time. This is performed by modeling and simulating a new system with $\frac{dv_{new}}{dt} = -\frac{dv_c}{dt}$ and $\frac{di_{new}}{dt} = -\frac{di_L}{dt}$ using Matlab Simulink to obtain the reverse time limit cycle. The variable d is defined by the boundary control law given in section 3.2.

The first boundary to be considered is $\theta_b = 115°$, which is the angular equivalent given by equation (3.2) for the $k = -2.2$ boundary used in [6], adjusting for the slightly different inductance and capacitance used in that reference. The separatrix for the boundary is shown in Figure 3.5.

The separatrix shown in Figure 3.5 defines the region of convergence for the ideal CPL synchronous buck converter being controlled by boundary control with $\theta_b = 115°$. Any initial operating point inside the region of convergence will converge to the desired operating point, while any initial operating point outside the separatrix will diverge to $v_C = 0$, at which point the singularity shown in (2.4) represents a nonphysical circuit condition for the ideal CPL model. Figure 3.5 also demonstrates that, unlike the asynchronous buck converter studied in [6], the boundary controlled synchronous buck converter region of convergence has an upper radial bound to stable operation in every angular direction.

Figure 3.6 shows the separatrix for other boundary angles $\theta_b = 100°$, $116°$, $120°$, and $130°$, demonstrating that the slope chosen for the boundary controller has an impact on the

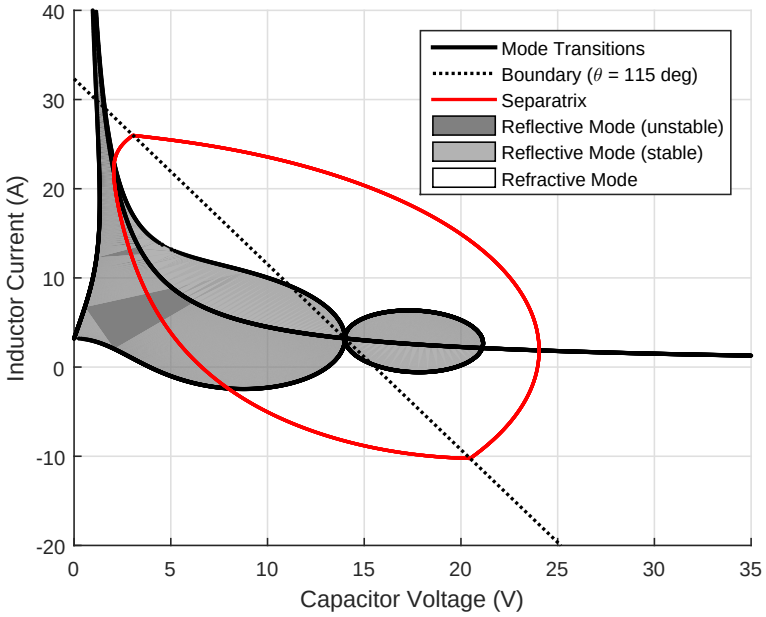
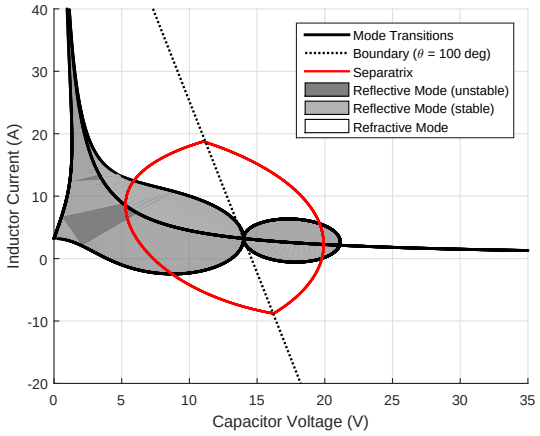


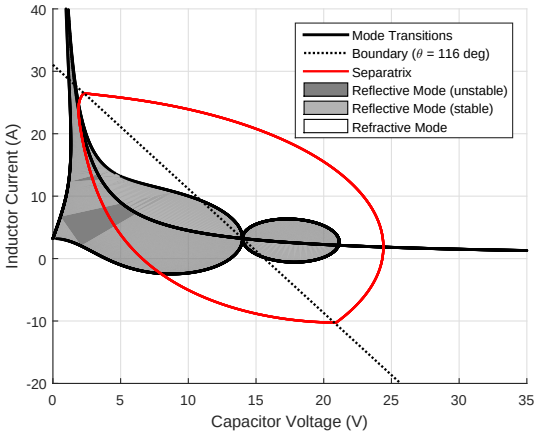
Figure 3.5: Boundary Control Separatrix Plot for $\theta_b = 115°$

region of convergence for the ideal CPL synchronous buck converter system model, which is not observed in asynchronous converters for boundary angles strictly between 90° and 116° due to the DCM. The separatrix for the 100° boundary shown in Figure 3.5 (a) demonstrates that boundaries with $\theta_b < 115°$ have a smaller region of convergence. Additionally, while the slight increase in minimum allowable voltage on the zero current axis shown in Figure 3.5 (d) for the 130° would discourage use of the boundary for an asynchronous converter, the increase in maximum voltage on the zero current axis for the synchronous configuration might be more important than the minimum voltage increase for some applications.

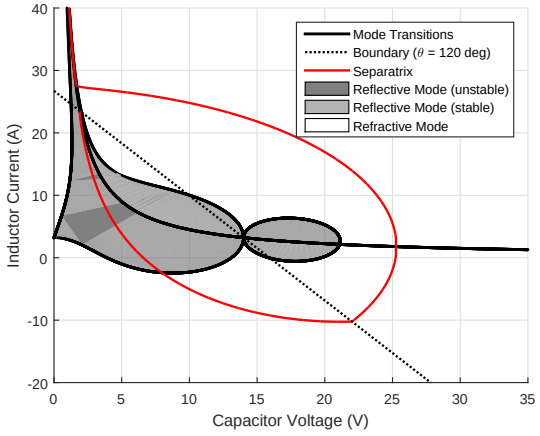
A feature of boundary control that is documented in [6, 9] and must be addressed in practical boundary control design is infinite frequency switching, or chattering, on stable reflective mode boundaries. To address this, hysteresis bands or timing restrictions can be used, and for the simulation controller model used in this chapter, a timing restriction in the form of a fixed controller sampling frequency was implemented. This boundary controller model was integrated into the model of (2.1) in MATLAB Simulink used in Chapter 2 for



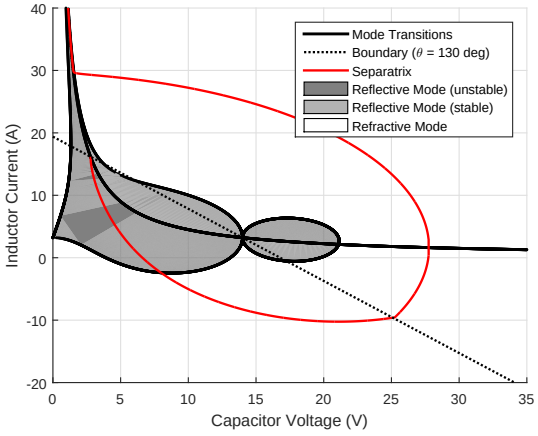
(a) $\theta_b = 100°$ Separatrix



(b) $\theta_b = 116°$ Separatrix



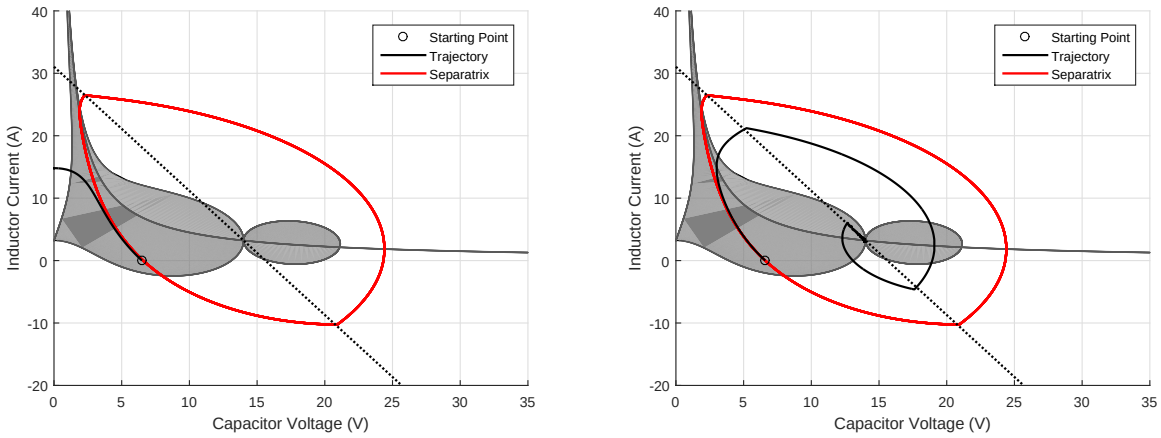
(c) $\theta_b = 120°$ Separatrix



(d) $\theta_b = 130°$ Separatrix

Figure 3.6: Boundary Control Separatrix Plots for θ_b = (a) 110°, (b) 116°, (c) 120° and (d) 130°.

constant duty cycle ideal CPL simulation. A figure of the resulting model is included in Appendix B in Figure B1. To verify the performance of the converter for the ideal CPL model, simulated converter trajectories for operation with the 116° boundary are shown for initial inductor current $i_L(0) = 0$ and initial capacitor voltages $v_C(0) = 6.5$ and $v_C(0) = 6.6$ in Figure 3.7.



(a) $v_C(0) = 6.5$; $i_L(0) = 0$ (b) $v_C(0) = 6.6$; $i_L(0) = 0$

Figure 3.7: Boundary Control Simulation State Space Trajectory Plots for (a) $v_C(0) = 6.5$; $i_L(0) = 0$ and (b) $v_C(0) = 6.6$; $i_L(0) = 0$. In both cases, $\theta_b = 116°$.

The simulation trajectory plots demonstrate that trajectories which start inside the separatrix converge to the operating point, while trajectories starting outside the separatrix end on the zero capacitor voltage axis.

Figure 3.8 shows the capacitor voltage and inductor current waveforms for $\theta_b = 116°$ with initial inductor current $i_L(0) = 0$ and initial capacitor voltage $v_C(0) = 6.6$.

The plot of the voltage and current allows for observation of the time it takes the system to converge to the desired operating point with a given control strategy, information which is not available from the state space trajectory plots which only plot current vs voltage, not time.

To verify the performance of the $\theta_b = 116°$ boundary controller for an LRC converter feeding a regulated POL converter, simulation voltage and current waveforms from the SimPowerSystems cascaded converter system model are presented in Figure 3.9. At $0.1s$ in the simulation, the voltage reference for the POL converter is increased from $0V$ to $5.83V$, corresponding to an attempted power increase from $0W$ to approximately $45W$.

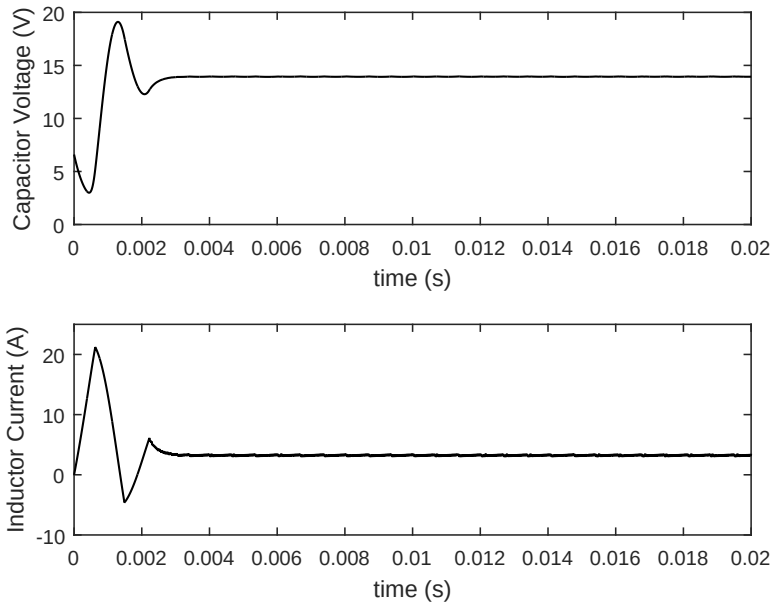
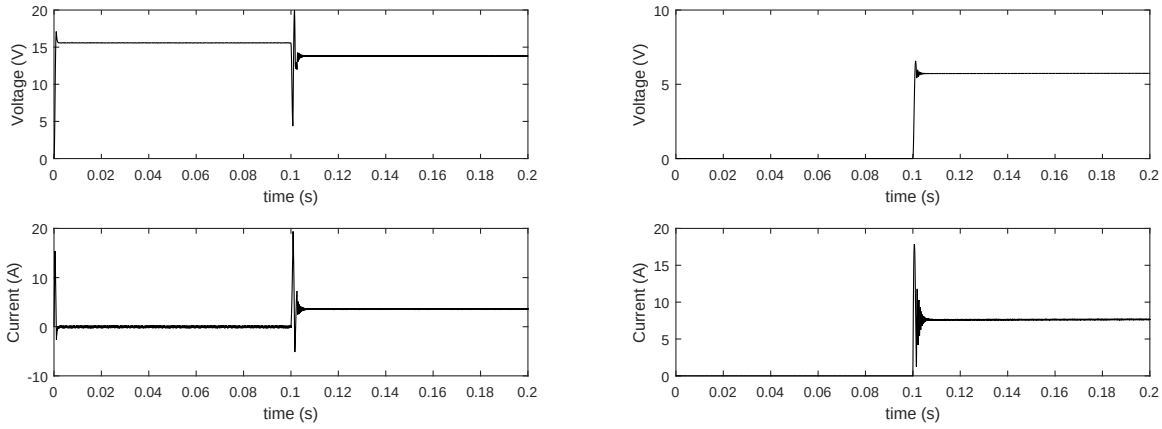


Figure 3.8: Boundary Control Simulation Capacitor Voltage and Inductor Voltage Waveforms for $v_C(0) = 6.6$; $i_L(0) = 0$ with $\theta_b = 116°$

Figure 3.9 (a) shows an initial transient as the LRC buck converter reaches steady state with $0W$ output power before $0.1s$ and a brief transient before reestablishing steady state operation after $0.1s$. Figure 3.9 (b) shows the simulation POL converter voltage and current waveforms, demonstrating that the POL converter is able to regulate its capacitor voltage near the voltage setpoint both after the step increase. The ability of the POL converter to regulate its load power indicates that it is an instantaneous CPL to the LRC converter, and the LRC is able to maintain stable operation.

The regions of convergence and the time it takes the system to converge to equilibrium are two controller performance criteria which can be used to measure the performance of the boundary controller to other control topologies.



(a) LRC Waveforms

(b) POL Waveforms

Figure 3.9: (a) LRC and (b) POL Converter Voltage and Current Waveforms for Simulation of Switching Model of the $\theta_b = 116^\circ$ Boundary Controlled Cascaded Converter System

4.0 PROPORTIONAL DERIVATIVE CONTROL OF CPL BUCK CONVERTERS

Proportional derivative (PD) control has been considered in [4] and [5] for the stabilization of the asynchronous buck converter with CPL. In this chapter, PD control is applied to the synchronous buck converter. Section 4.1 gives an introduction to PD control for power electronic converters and discusses the work of the two references mentioned above and how the results apply to the synchronous configuration, Section 4.2 presents a small-signal stability analysis using the methods of linear controls, Section 4.3 uses state space geometrical arguments from boundary control to provide design insight into the PD controller parameter choice, and Section 4.4 presents simulation results for both ideal CPL synchronous buck converter and cascaded converter systems supporting the analysis.

4.1 INTRODUCTION TO PROPORTIONAL DERIVATIVE CONTROL

For PD control, the duty cycle control law is (4.1), where $e := V_{ref} - v_c$.

$$d = k_d\dot{e} + k_p e + D \tag{4.1}$$

In [5], passivity-based control (PBC) is used to prove global stability of the closed-loop system with the set of PD controller coefficients defined by (4.2) if the controller action is unconstrained.

$$k_d = \frac{R_1 C}{E};\; k_p = \frac{R_1}{R_2 E};\; R_1 > 0;\; R_2 > 0 \tag{4.2}$$

The parameters R_1 and R_2 in (4.2) correspond to adding a virtual resistance in series with the inductor and in parallel with the capacitor, respectively, allowing a more intuitive

way of understanding the PD parameters k_d and k_p, however the proof of global stability relies on an unconstrained duty cycle, and only local stability is achieved once the duty cycle is constrained to $0 < d < 1$ [5]. [4] relies on system trajectory analysis rather than mathematical stability proofs to analyze the large signal stability and region of convergence of the converter, and those trajectory arguments are what [5] uses once the saturated control action is accounted for.

Before using simulation to examine the large-signal system trajectories of the PD compensated synchronous buck converter with CPL, however, a small-signal justification for pursuing PD control will be presented.

4.2 SMALL-SIGNAL STABILITY ANALYSIS OF PD COMPENSATED CPL BUCK CONVERTER

From the system of differential equations for the ideal CPL synchronous buck converter system in (2.10), a first-order linear approximation for operation around the desired operating point given in (2.9) can be obtained. The resulting system of linear differential equations is (4.3).

$$\begin{aligned} \frac{d\widetilde{v_C}}{dt} &\approx \frac{1}{C}\left(\widetilde{i_L} + \frac{P_L}{\overline{v_C}^2}\widetilde{v_C}\right) \\ \frac{d\widetilde{i_L}}{dt} &\approx \frac{1}{L}\left(\widetilde{d}E - \widetilde{v_C}\right) \end{aligned} \tag{4.3}$$

The Laplace transform can be applied to (4.3) after assuming equality. Assuming zero initial conditions, the plant transfer function from $\widetilde{d}(s)$ to $\widetilde{v_C}(s)$ is given by (4.4).

$$G_p(s) := \frac{\widetilde{v_C}(s)}{\widetilde{d}(s)} = \frac{\frac{E}{LC}}{s^2 - \left(\frac{P_L}{C\overline{v_C}^2}\right)s + \frac{1}{LC}} \tag{4.4}$$

As the coefficient of s is negative while the coefficients of s^2 and 1 are positive in the denominator of $G_p(s)$, the poles of the transfer function are in the right half plane and thus that the plant is unstable. Using the PD control law given in (4.1), the compensator transfer function from $e(s)$ to $\widetilde{d}(s)$ is given in (4.5).

$$G_c(s) := \frac{\widetilde{d}(s)}{e(s)} = k_d s + k_p \tag{4.5}$$

Figure 4.1 gives the block diagram for the connection of $G_c(s)$ and $G_p(s)$ to represent the small-signal linearized model of the PD-compensated ideal CPL synchronous buck converter system.

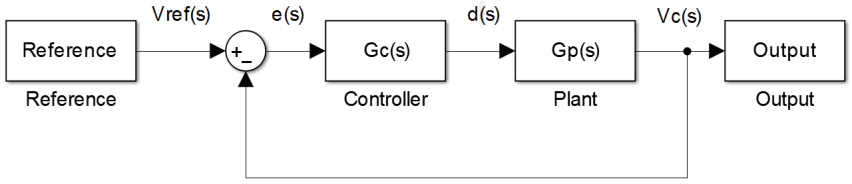


Figure 4.1: Block diagram for PD compensated converter

From the block diagram, converter transfer function (4.4), and compensator transfer function (4.5), the closed loop transfer function from $V_{ref}(s)$ to $V_c(s)$ is given in (4.6).

$$T(s) := \frac{\widetilde{v_c}(s)}{V_{ref}(s)} = \frac{G_c(s)G_p(s)}{1 + G_c(s)G_p(s)} = \frac{(k_d E)s + k_p E}{(LC)s^2 + \left(k_d E - \frac{LP_L}{\overline{v_c}^2}\right)s + (k_p E + 1)} \tag{4.6}$$

From closed-loop transfer function $T(s)$, criteria for controller gains k_p and k_d which will result in left half plane poles and stable operation can be determined. A controller with parameters meeting the criteria would give stable operation of the small-signal linearized model in Figure 4.1. For the roots of the second order denominator polynomial in s to be in the left half plane, having negative real parts, the Routh-Hurwitz Criterion requires all three denominator coefficients to be of the same sign [11]. As the coefficient of s^2 is +1, this gives the requirements in (4.7) for the other two coefficients to positive.

$$k_p > -\frac{1}{E};\ k_d > \frac{LP_L}{E\overline{v_C}^2} \tag{4.7}$$

If parameters are chosen that satisfy these criteria, the system will be locally stable in a region around the operating point where neither duty cycle saturation nor errors resulting from linearization impact the system substantially. In particular, we see that the proportional action of the controller is not necessary for small-signal stability as $k_p = 0$ meets the minimum gain requirement. The derivative action of the controller is necessary for small-signal stability, however, with a minimum derivative gain of $k_d = \frac{LP_L}{E\overline{v_C}^2}$. The small-signal stability analysis gives no information about the effects of the duty cycle being constrained to the range $0 < d < 1$, however, nor does it give information about global stability concerns or the region of convergence. For insight into these concerns, Section 4.3 will focus on graphical and geometrical analysis of the PD control strategy while Section 4.4 will show the behavior of the system through simulation.

4.3 GEOMETRICAL AND LARGE-SIGNAL ANALYSIS OF PD COMPENSATED CPL BUCK CONVERTER

In Chapter 3, it was demonstrated how boundary control uses a geometrical surface to define the switching action of a converter. In the buck converter case considered, $d = 0$ in the region above the boundary, while $d = 1$ below the boundary. Once the state reaches the boundary in the reflective region, the converter operation remains on the boundary with duty cycle given by (3.5).

In PD control, the control law determines the duty cycle for the converter, which determines the switching action of the converter. Using the fast-averaged model of the ideal CPL synchronous buck converter in (2.8) and the PD control law in (4.1), the controller duty cycle output can be found as the function of the capacitor voltage v_C and inductor current i_L given in (4.8).

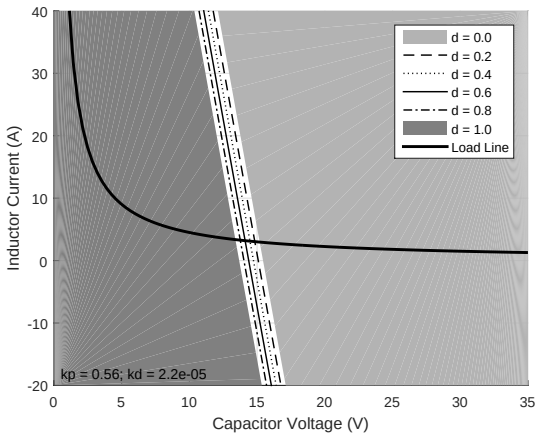
$$d = \frac{k_d}{C}\left(\frac{P_L}{v_C} - i_L\right) + k_p\left(V_{ref} - v_c\right) + D \tag{4.8}$$

(4.8) can be solved for the inductor current as a function of the duty cycle and the capacitor voltage as given in (4.9), allowing the mapping of the duty cycle given by the controller to the voltage and current state space to visualize the effects of saturation in PD control of the system.

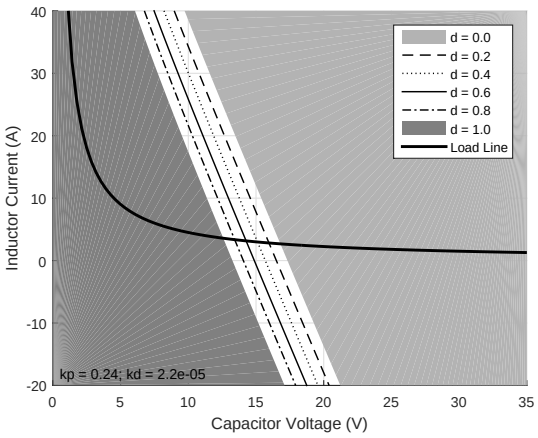
$$i_L = \frac{C}{k_d}(D-d) + \frac{P_L}{v_C} + \frac{k_p C}{k_d}\left(V_{ref} - v_c\right) \tag{4.9}$$

(4.8) demonstrates that higher controller gains will lead to increased saturation. With high enough gains, the controller saturation leads to PD control operating essentially as boundary control. (4.9) gives the shape of the contours in the state space where the controller will produce a given duty cycle. The $\frac{k_p C}{k_d}\left(V_{ref} - v_c\right)$ term gives a linear contribution to the contour with slope $-\frac{k_p C}{k_d}$, while the $\frac{P_L}{v_C}$ term gives a nonlinear contribution equal in current magnitude to the CPL current at a given voltage. Using (4.9), duty cycle maps are presented in Figure 4.2 for the two sets of controller parameters used in [5], which are defined by (4.2) using $R_1 = 1$; $R_2 = 0.085$ and $R_1 = 1$; $R_2 = 0.2$. The maps shown in Figure 4.3 are for cases with no proportional gain and derivative gains corresponding to $R_1 = 0.2442$; $R_2 = \infty$ and $R_1 = 1$; $R_2 = \infty$. $R_1 = 0.2442$; $R_2 = \infty$ corresponds approximately to the lowest derivative gain allowed by (4.7) for stable operation of the small-signal linearized model.

As demonstrated by Figure 3.6 in Section 3.3, steeper boundaries in boundary control tend to lead to smaller regions of convergence. With this in mind, it can reasonably be expected that the PD parameters mapped in Figure 4.2 (a) will have a smaller region of convergence than those mapped in Figure 4.2 (b), and it may be possible to increase the region of convergence by adjusting the slope even further by reducing or eliminating k_p. Examining the implementation of these considerations, as well as examining the effects of varying the gains to reduce or increase saturation as seen by comparing Figure 4.3 (a) with (b), will be the focus of the simulations presented in Section 4.4.

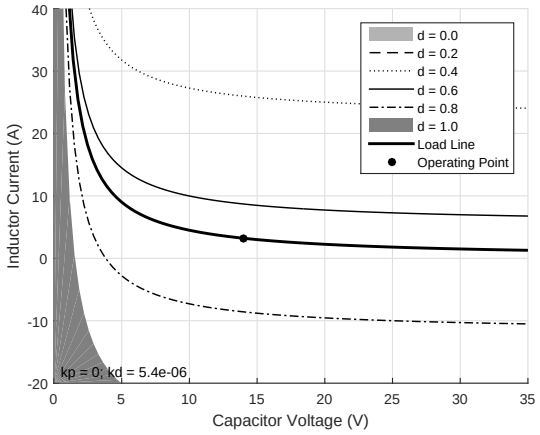


(a) $R_1 = 1$; $R_2 = 0.085$

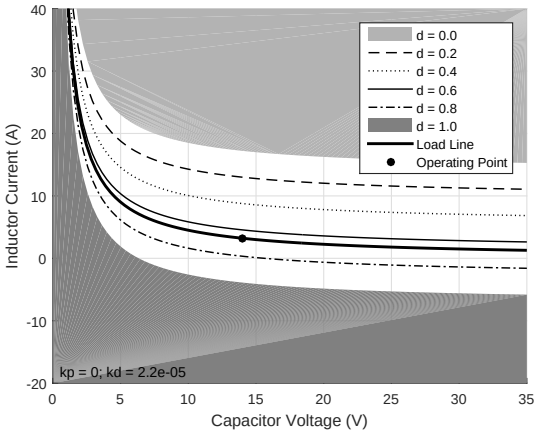


(b) $R_1 = 1$; $R_2 = 0.2$

Figure 4.2: PD Duty Cycle Plots for (a) $R_1 = 1$; $R_2 = 0.085$ and (b) $R_1 = 1$; $R_2 = 0.2$



(a) $R_1 = 0.2442$; $R_2 = \infty$



(b) $R_1 = 1$; $R_2 = \infty$

Figure 4.3: PD Duty Cycle Plots for (a) $R_1 = 0.2442$; $R_2 = \infty$ and (b) $R_1 = 1$; $R_2 = \infty$

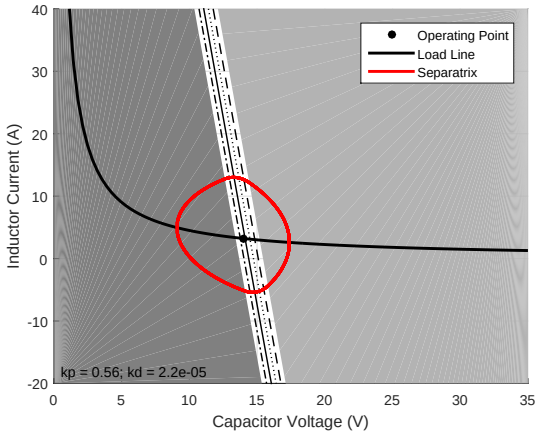
4.4 SIMULATION RESULTS WITH PD CONTROL

As with the consideration of boundary control using simulation in Section 3.3, the separatrix for the CPL synchronous buck converter system can be obtained from numerical simulation of the differential equations from (2.8) in reverse time. The duty cycle variable d is defined by the PD control law (4.1), with the necessary change that the derivative $\dot{e}$ is replaced by $-\dot{e}$ for reverse time simulation. Figure 4.4 (a) and (b) give the separatrix for the controller parameters considered in Figure 4.2, while Figure 4.4 (c) and (d) show the separatrix for the minimum k_d case in Figure 4.3 (a).

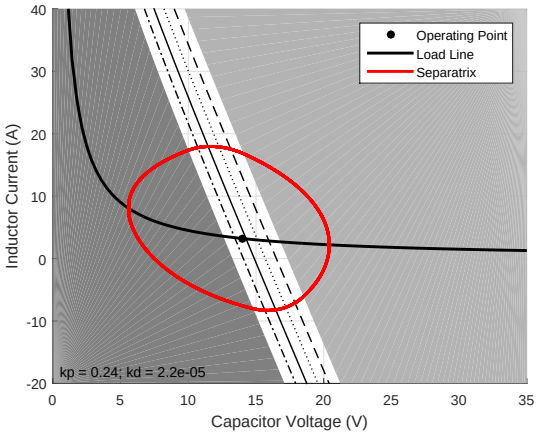
The separatrix for each of the cases in Figure 4.4 (a) and (b) show the PD parameters chosen in [5] can be expected to give a smaller region of convergence for the synchronous buck converter than the boundary controller from [6] examined in Figure 3.5. The separatrix shown for k_d of approximately the minimum stable value indicated in Section 4.2 shows a negligible region of convergence, indicating a larger value of k_d must be used in practical controller design.

Figure 4.5 (a) and (b) show separatrix plots for two cases with $k_p = 0$ and larger values of k_d. Figure 4.5 (a) shows the separatrix for the $R_1 = 1$ case considered in 4.3 (b), while Figure 4.5 (b) considers $R_1 = 10$.

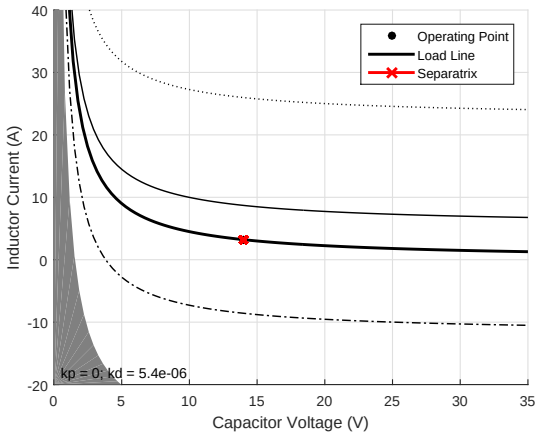
Purely judging the performance of the controller parameter sets corresponding to Figure 4.5 based on the simulation region of convergence, the higher k_d value in Figure 4.5 (b) does seem to improve the region of convergence compared to Figure 4.5 (a). However, it can be seen that the higher k_d gain also results in increased controller saturation. From practical design considerations, we also know that higher values k_d will amplify any noise more, which can be detrimental to system performance. Also to be considered is the difference differing gain values may have on the speed of convergence to the operating point. This last question will be examined for the gain parameters examined in 4.5 (a) and (b) by plotting the state space trajectories and waveforms for voltage and current of the system starting at the same initial condition for the two controller parameter sets. Figure 4.6 (a) and (c) show these



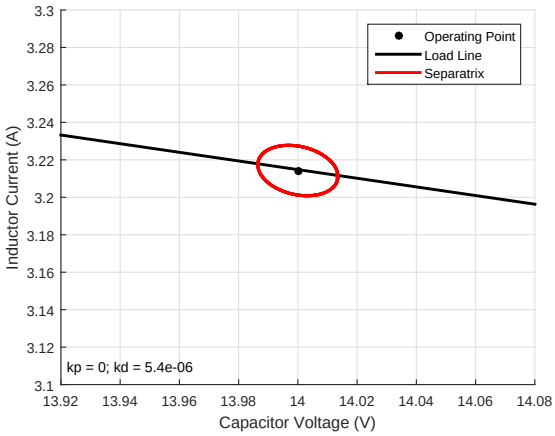
(a) $R_1 = 1$; $R_2 = 0.085$



(b) $R_1 = 1$; $R_2 = 0.2$



(c) $R_1 = 0.2442$; $R_2 = \infty$

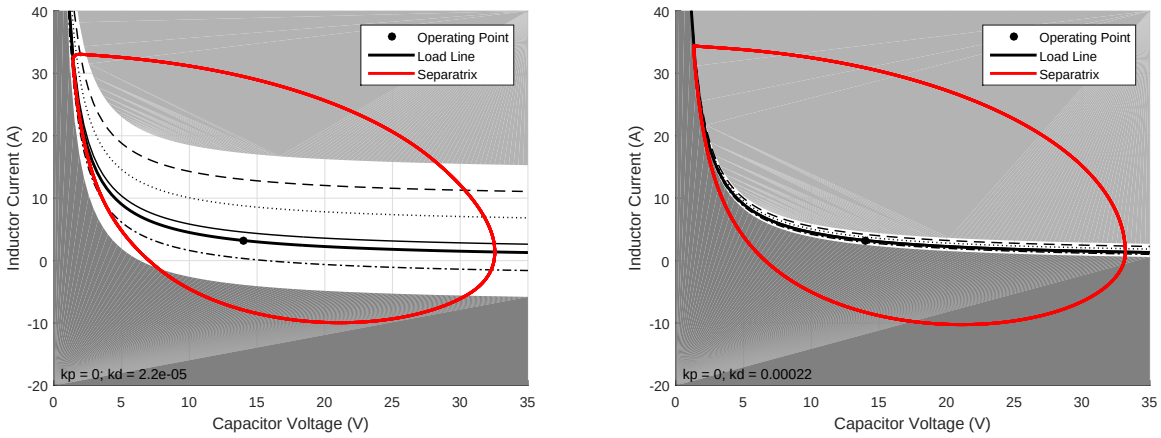


(d) $R_1 = 0.2442$; $R_2 = \infty$ OP Close-up

Figure 4.4: PD Separatrix Plots for (a) $R_1 = 1$; $R_2 = 0.085$, (b) $R_1 = 1$; $R_2 = 0.2$, (c) $R_1 = 0.2442$; $R_2 = \infty$, and (d) $R_1 = 0.2442$; $R_2 = \infty$ Operating Point Close-up

plots for $R_1 = 1$, while (b) and (d) show the plots for $R_1 = 10$. A figure of the MATLAB Simulink model of the PD compensated ideal CPL synchronous buck converter model used for these simulations is included in Appendix B in Figure B1.

Figure 4.6 demonstrates that though increasing the derivative gain can tend to lead to an increased region of convergence for the system, beyond the critical damping point increasing



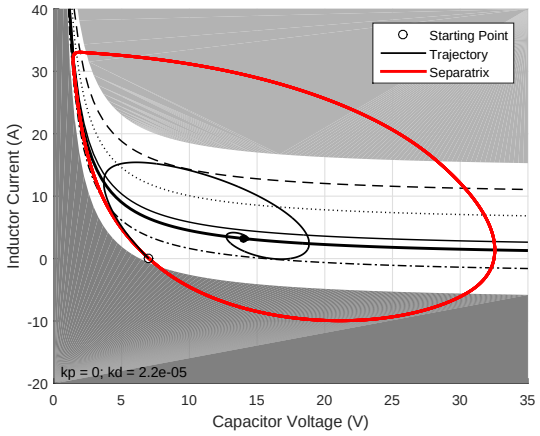
(a) $R_1 = 1;\ R_2 = \infty$ (b) $R_1 = 10;\ R_2 = \infty$

Figure 4.5: PD Separatrix Plots for (a) $R_1 = 1;\ R_2 = \infty$ and (b) $R_1 = 10;\ R_2 = \infty$

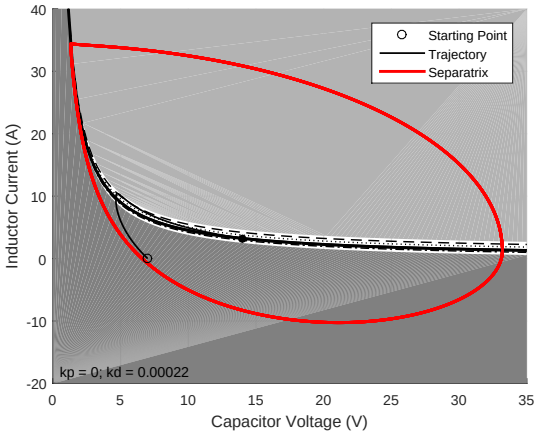
the gain also tends to lead to slower, overdamped system response. The response for $R_1 = 1$ in this case is underdamped and exhibits an overshoot, however, which in some applications may be an undesired condition. Even if overshoot is unacceptable, however, the damping produced by $R_1 = 10$ is likely excessive and the gains could be fine-tuned to produce a faster, critically damped response. Small-signal root locus or frequency domain techniques may be of use for fine-tuning the parameters, however the effects of controller saturation and system nonlinearities would also need to be considered. The optimal tuning of the parameters is beyond the scope of this thesis.

To verify the performance of the PD controller for an LRC converter feeding a regulated POL converter, simulation voltage and current waveforms from the SimPowerSystems cascaded converter system model with the $R_1 = 10$ PD controller are presented in Figure 4.7. At $0.1s$ in the simulation, the voltage reference for the POL converter is increased from $0V$ to $5.83V$, corresponding to an attempted power increase from $0W$ to approximately $45W$.

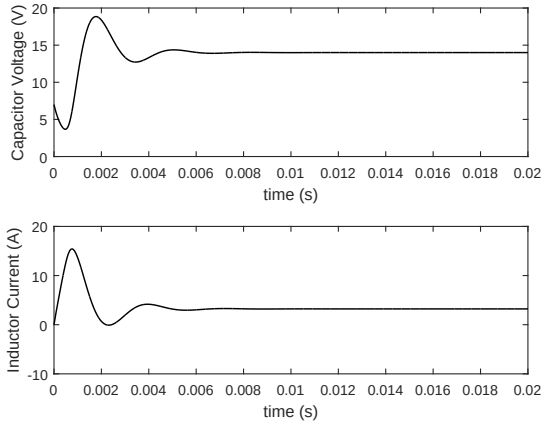
Figure 4.7 (a) shows an initial transient as the LRC buck converter reaches steady state with $0W$ output power before $0.1s$ a brief transient before reestablishing steady state operation after $0.1s$. Figure 4.7 (b) shows the simulation POL converter voltage and current



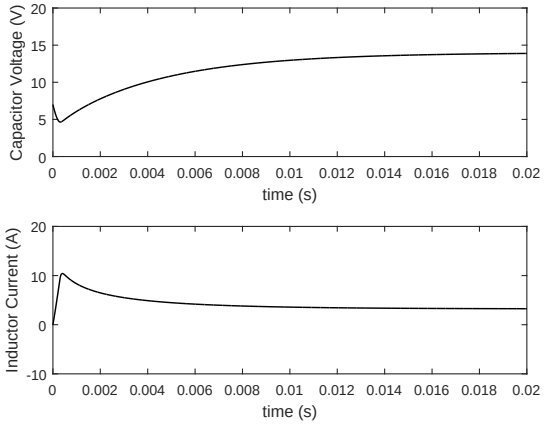
(a) $R_1 = 1$; $R_2 = \infty$ State Space Trajectory



(b) $R_1 = 10$; $R_2 = \infty$ State Space Trajectory



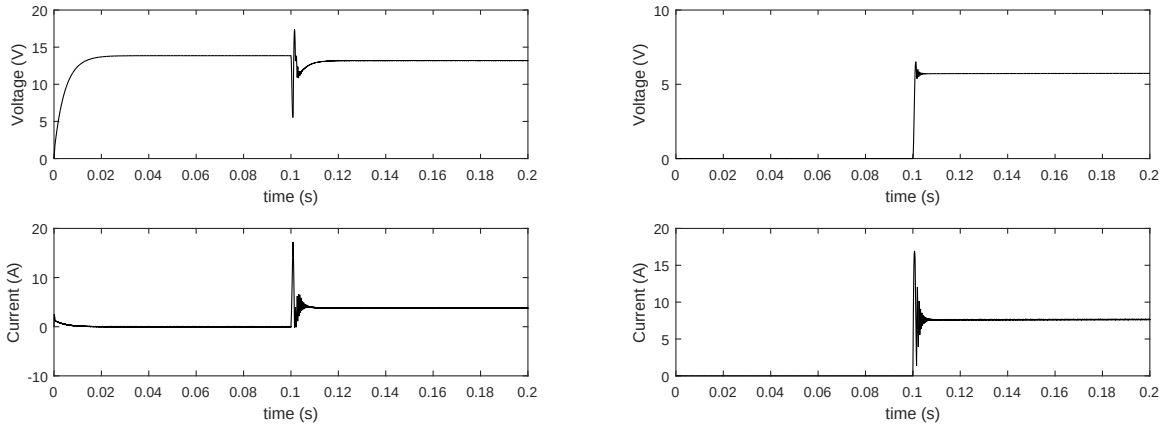
(c) $R_1 = 1$; $R_2 = \infty$ Waveforms



(d) $R_1 = 10$; $R_2 = \infty$ Waveforms

Figure 4.6: PD State Space Trajectory Plots for (a) $R_1 = 1$; $R_2 = \infty$, (b) $R_1 = 10$; $R_2 = \infty$ and Waveforms for (c) $R_1 = 1$; $R_2 = \infty$, (d) $R_1 = 10$; $R_2 = \infty$. In all cases, $v_C(0) = 7V$; $i_L(0) = 0$

waveforms, demonstrating that the POL converter is able to regulate its capacitor voltage near the voltage setpoint both before after the step increase. The ability of the POL converter to regulate its load power indicates that it is an instantaneous CPL to the LRC converter, and the PD compensated LRC is able to maintain stable operation.



(a) LRC Waveforms

(b) POL Waveforms

Figure 4.7: (a) LRC and (b) POL Converter Voltage and Current Waveforms for Simulation of Switching Model of $R_1 = 10$; $R_2 = \infty$ PD Controlled Cascaded Converter System

5.0 PROPORTIONAL INTEGRAL DERIVATIVE CONTROL OF CPL BUCK CONVERTERS FOR VOLTAGE REGULATION

Assuming both the load power and source voltage are known and constant, the boundary control examined in Chapter 3 and the PD control examined in Chapter 4 can stabilize the ideal CPL synchronous buck converter at the desired voltage reference. However, if load power or source voltage change or if circuit parameters or losses are inaccurately accounted for, voltage error will result. Both [5] and [6] recognize this and propose regulation of the voltage using an integral controller action.

The regulation of voltage using a proportional integral (PI) controller to regulate the current set point for the boundary controlled asynchronous buck converter was demonstrated experimentally in [6] for the case of a change in load power, but the stability of the controller was not mathematically proven. The cascaded combination of PI control with boundary control of a nonlinear system make analysis particularly challenging.

Likewise, the addition of an integral component to the PD control derived using passivity based control techniques in [5] was not included in the mathematical proofs of stability, but the use of PID control for the asynchronous buck converter with CPL is nevertheless supported by experimental experience and simulation results.

In this chapter, a linearized small-signal analysis of PID control for the ideal CPL synchronous buck converter analogous to that presented for PD control in Section 4.2 is given in Section 5.1, followed by simulation results in Section 5.2 examining controller performance for both ideal CPL and cascaded converter system models.

5.1 SMALL-SIGNAL STABILITY ANALYSIS OF PID COMPENSATED CPL BUCK CONVERTER

The small-signal transfer function for the converter was given in (4.4) and is duplicated in (5.1), while the PID control law for the duty cycle is given in (5.2).

$$G_p(s) = \frac{\frac{E}{LC}}{s^2 - \left(\frac{P_L}{C\overline{v_C}^2}\right)s + \frac{1}{LC}} \tag{5.1}$$

$$d = k_p e + k_i \int e + k_d \dot{e} + D \tag{5.2}$$

Using the control law given in (5.2), the compensator transfer function is (5.3).

$$G_c(s) = k_p + \frac{k_i}{s} + k_d s \tag{5.3}$$

Using converter transfer function (5.1) and compensator transfer function (5.3), the closed loop transfer function of the system shown in Figure 4.1 is (5.4).

$$T(s) := \frac{(k_d E)s^2 + (k_p E)s + k_i E}{(LC)s^3 + \left(k_d E - \frac{LP_L}{\overline{v_c}^2}\right)s^2 + (k_p E + 1)s + k_i E} \tag{5.4}$$

In Section 4.2, the Routh Hurwitz criterion was used to produce requirements for the compensator gains for left half plane roots of the characteristic polynomial. The criterion can be applied to a third-order polynomial also, but the resulting criteria differ as a result of the higher order. The criteria for all roots of arbitrary third-order polynomial $a_3 s^3 + a_2 s^2 + a_1 s + a_0 = 0$ with $a_3 > 0$ to be in the left half plane are as given in (5.5) [11].

$$a_3 > 0;\ a_2 > 0;\ a_1 > \left(\frac{a_3 a_0}{a_2}\right);\ a_0 > 0 \tag{5.5}$$

Applying (5.5) to the characteristic equation of transfer function (5.4), the requirements for the PID compensator gains are given in (5.6).

$$k_p > -\frac{1}{E};\ k_d > \frac{LP_L}{E\overline{v_C}^2};\ k_i < \left(k_p + \frac{1}{E}\right)\left(\frac{k_d E - \frac{LP_L}{\overline{v_C}^2}}{LC}\right) \tag{5.6}$$

The requirements obtained in (5.6) place an upper bound on the integral gain and place the same lower bound requirements on proportional and derivative gains as was determined

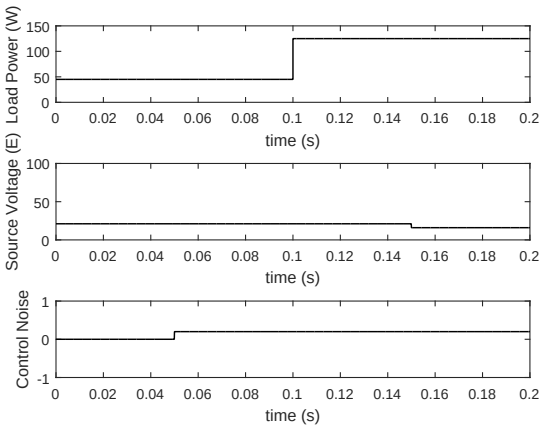
for PD compensation in (4.7). The PD simulation results in section 4.4 indicated smaller positive values of proportional gain tended to produce larger regions of convergence, suggesting the consideration of the $k_p = 0$ may again prove useful. If $k_p = 0$, the upper bound on the integral gain is given by $k_{i;\,max} = (1/(LC))(k_d - (LP_L)/(E\overline{v_C}^2))$. It can further be observed that the bounds on the derivative and integral gains are more severe for increased values of P_L and decreased values of E, indicating that if a compensator is to be designed for a range of load powers and source voltages, the maximum load power and minimum source voltage should be the values used in compensator parameter design.

The performance of the system with PID compensation through disturbances to load power, line voltage, and duty cycle error will be observed through simulation in Section 5.2.

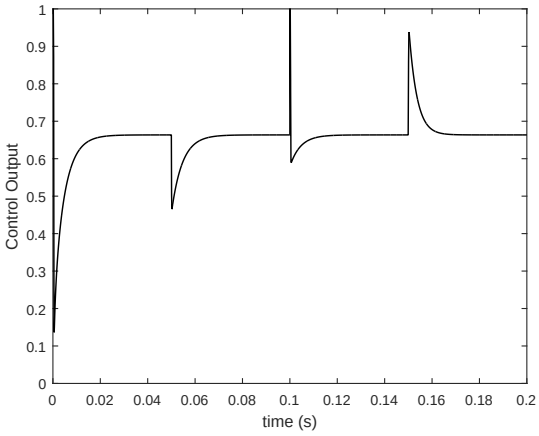
5.2 SIMULATION RESULTS WITH PID CONTROL

To this point in this thesis, constant duty cycle error of 0, constant load power of 45W, and constant line voltage of 21.1 V have been used in analysis and simulation. To examine the performance of the PID compensated ideal CPL synchronous buck converter mathematical model with disturbances, however, a $0.2s$ simulation with a step increase in duty cycle error from 0 to 0.2 at $0.05s$, a step increase in load power from $45W$ to $125W$ at $0.1s$, and a step decrease in line voltage from $21.1V$ to $16V$ at $0.15s$ will be used. With $P_{L;\,max} = 125W$ and $E_{min} = 16V$, $k_{d;\,min} = 1.993 * 10^{-5}$ and $R_{1;\,min} = 0.8947$. Choosing $R_1 = 10$ and $R_2 = \infty$ so the system displays an overdamped response that results in cleaner plots, as used in Figure 4.6 (b) and (d), the maximum integral gain $k_{i;\,max} = 863.06$. For comparison, simulation results for $k_i = 0$ are presented in Figure 5.1, and results for $k_i = 10$ are given in Figure 5.2. Results are from simulation of the MATLAB Simulink model shown in Appendix B in Figure B3.

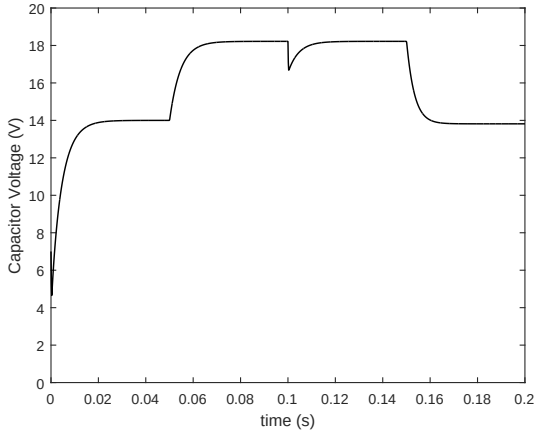
Figure 5.1 (c) shows that in fact, changes in load power do not impact the output voltage of the model used because no resistive losses are accounted for. However, without integral controller action, it is demonstrated that disturbances in source voltage or errors in the



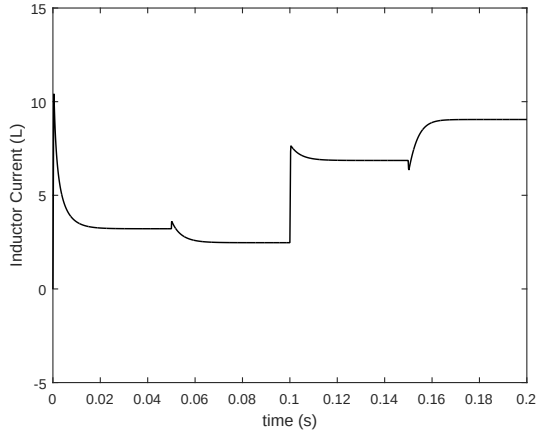
(a) Disturbances



(b) Control Output



(c) Capacitor Voltage

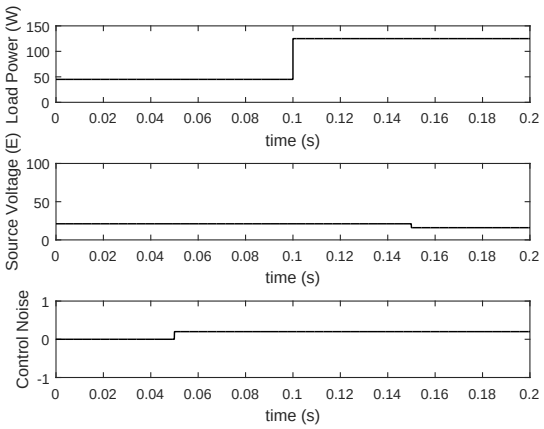


(d) Inductor Current

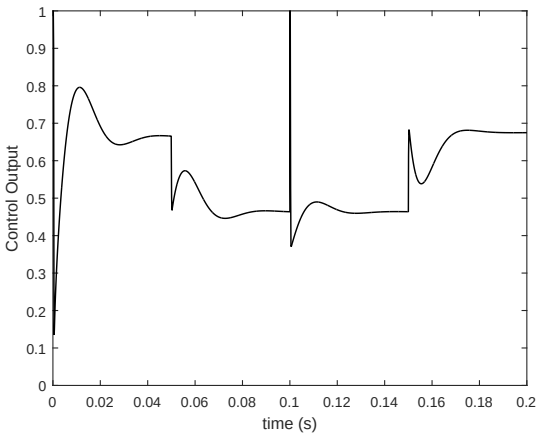
Figure 5.1: Plots of (a) Disturbances, (b) Controller Duty Cycle Output, (c) Capacitor Voltage, and (d) Inductor Current for $R_1 = 10$, $R_2 = \infty$, and $k_i = 0$.

control signal have a significant effect on the output voltage. Figure 5.2 (c) demonstrates that integral compensation in the PID controller is able to correct for the source voltage and control signal disturbances.

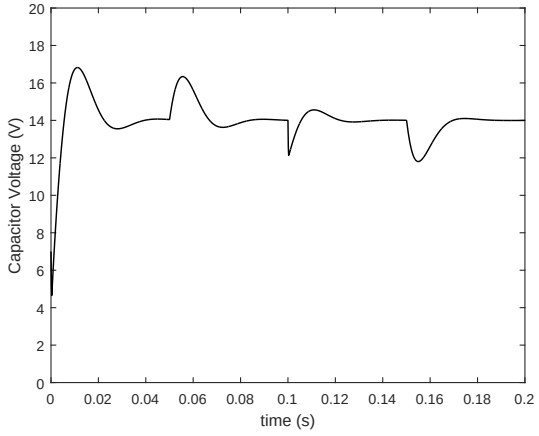
The addition of disturbances means that even if the separatrix were to be plotted, each set of disturbance values would have a unique separatrix, complicating the determination of



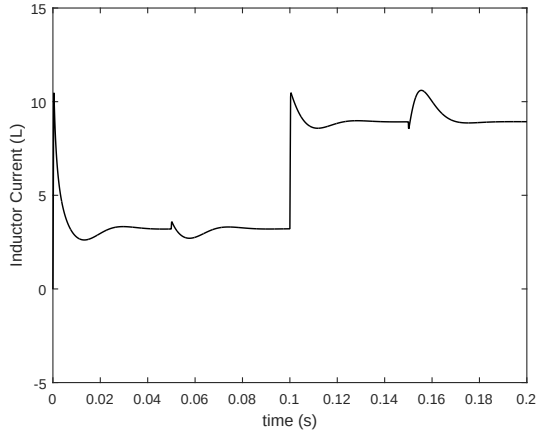
(a) Disturbances



(b) Controller Output



(c) Capacitor Voltage



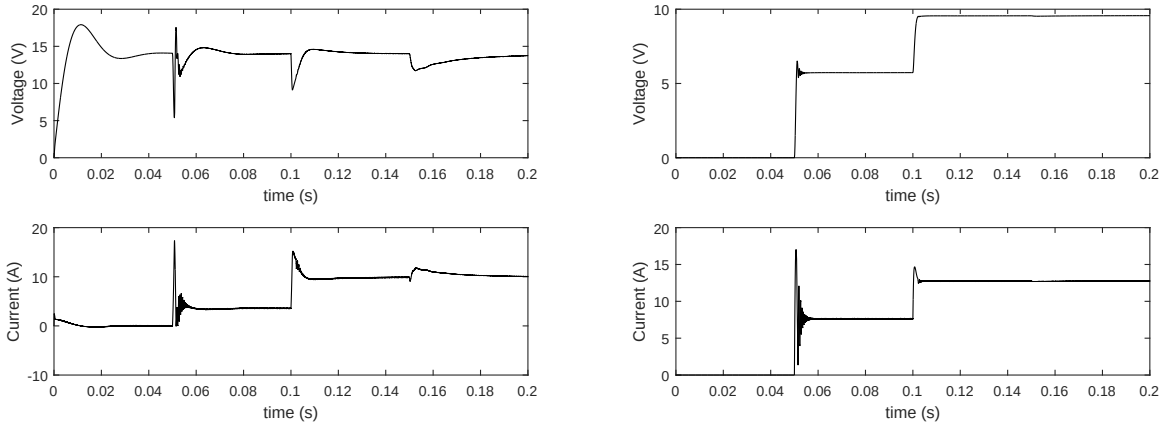
(d) Inductor Current

Figure 5.2: Plots of (a) Disturbances, (b) Controller Duty Cycle Output, (c) Capacitor Voltage, and (d) Inductor Current for $R_1 = 10$, $R_2 = \infty$, and $k_i = 10$.

the region of convergence over all operating conditions. However, because the addition of the integral compensation also causes the system to not be memoryless, the separatrix for the PID compensated system cannot be plotted through simulation in the same manner as

was done in Sections 3.3 and 4.4 even without disturbances, and the plots therefore show only specific results from the set of simulations performed without the region of convergence information included in plots in the previous chapters.

To verify the performance of the PID controller for an LRC converter feeding a regulated POL converter with disturbances, simulation voltage and current waveforms from the SimPowerSystems cascaded converter system model with the $R_1 = 10$, $R_2 = \infty$, and $k_i = 10$ PID controller are presented in Figure 5.3. A step increase in voltage for the POL converter from $0V$ to $5.83V$ occurs at $0.05s$ corresponding to an attempted power increase from $0W$ to approximately $45W$, a further step increase in voltage for the POL converter from $5.83V$ to $9.68V$ occurs at $0.10s$ corresponding to an attempted power increase from $45W$ to approximately $125W$, and a step decrease in source voltage from $21.1V$ to $16V$ occurs at $0.15s$.



(a) LRC Waveforms

(b) POL Waveforms

Figure 5.3: (a) LRC and (b) POL Converter Voltage and Current Waveforms for Simulation of Switching Model of $R_1 = 10$; $R_2 = \infty$; $k_i = 10$ PID Controlled Cascaded Converter System With Disturbances

Figure 5.3 (a) shows an initial transient as the LRC buck converter reaches steady state with $0W$ output power before $0.05s$ and transients before reestablishing steady state operation following each disturbance. Figure 5.3 (b) shows the simulation POL converter voltage

and current waveforms, demonstrating that the POL converter is able to regulate its capacitor voltage near the voltage setpoint after each step increase. The ability of the POL converter to regulate its load power indicates that it is an instantaneous CPL to the LRC converter, and the PD compensated LRC is able to maintain stable operation.

6.0 CONCLUSIONS

This thesis has examined the effects of CP load characteristics on the operation of the synchronous buck dc-dc converter. With an ideal CPL, the synchronous buck converter under constant duty cycle operation fails to converge either to equilibrium or to any limit cycle, diverging for all nonequilibrium initial conditions. With a tightly regulated POL converter, an LRC synchronous buck converter under constant duty cycle operation does not diverge but exhibits oscillatory limit cycle behavior, with the LRC output voltage passing below the minimum CP voltage of the POL converter in each cycle. Unlike the asynchronous buck converter, no intrinsic DCM exists to force limit cycle behavior in the synchronous buck converter with CPL, and the limit cycle only occurs because the POL converter is unable to regulate its output voltage when the LRC converter output voltage drops below the minimum voltage for CP load behavior.

Before examining control strategies, a polar coordinate mathematical model of the ideal CPL buck converter has been derived that allows for proof of global absence of convergence with constant duty cycle and a direct energy based measure of the distance from the desired operating point. This modeling technique makes use of the oscillatory exchange of energy between the inductor and capacitor to treat the periodic oscillations as an orbit and may be of future interest in the study of analysis or control of dc-dc converters.

Geometrical boundary control and PD control have both been considered to stabilize the ideal CPL buck converter and the cascaded converter systems. The analysis and design of the boundary controller in the polar coordinate representation presented provides an alternative to the rectangular coordinate methods cited. The region of convergence and

local stabilization of the system under boundary control have been verified using numerical simulation for both the mathematical model of the ideal constant power load system and the component model of the cascaded system. The analysis and design of the PD controller presented uses both small-signal techniques and geometrical insights from boundary control, and the region of convergence and local stabilization have been verified using simulation. While the small-signal techniques are able to determine controller parameter criteria for local stability, the geometrical examination of the duty cycle points towards setting the proportional gain to zero for improved region of convergence and gives a graphical presentation of the dependence of the regions of controller saturation on the derivative gain. The region of convergence and local stabilization of the system under PD control have been verified using numerical simulation for both the mathematical model of the ideal constant power load system and the component model of the cascaded system in the same way as for boundary control. Lastly, the addition of an integral component to the PD controller to compensate for operating point changes, control signal error, and parameter uncertainty has been analyzed using small-signal techniques, with the performance of the system models under PID control verified through simulation.

The choice between the control strategies studied in this thesis is not clear cut and depends both on the application and performance metrics considered. Boundary control intrinsically treats the converter as a switching system and, in that sense, is more naturally suited to switched power converters than linear control methods are. Boundary control also tends to be robust to variations in component parameters or source voltage; however, unless the controller is augmented with additional regulation, changes in load power from the design point introduce a steady-state voltage error. PD control, in contrast, is a linear control strategy being applied to a switched and intrinsically nonlinear system. While the ideal PD control performs very well in simulation, in real applications the derivative component of the control tends to be susceptible to noise and likely requires additional filtering to perform well. The PD control also is sensitive to circuit losses and variations in component parameters or source voltage unless an integral component is added to the control law, though changes in load power do not cause any steady-state voltage error unless circuit losses are considered. If disturbance rejection is required, analysis of PID control is more

straightforward than analysis of a PI compensator cascaded with a boundary controller, which may be an important consideration in favor of linear controls until stability of the cascaded boundary control can be analytically demonstrated.

Finally, this thesis would be incomplete if some comments on the stability challenges the synchronous buck converter has in comparison with the asynchronous buck converter were not made. Throughout this thesis, it has been noted that the absence of intrinsic DCM operation in the synchronous converter eliminated the open loop stable limit cycle of the ideal CPL buck converter system and only allows the cascaded system to converge to limit cycle behavior by leaving the POL converter CP voltage range. In addition, without DCM operation, controllers for the synchronous buck converter with ideal CPL have upper radial bounds to the region of convergence around the equilibrium point in all directions rather than simply a minimum voltage for stable operation. In summary, both controlled and uncontrolled, the synchronous buck converter with CPLs is less intrinsically stable than the asynchronous buck converter, and this may be an additional consideration in the choice of converter topology for power electronic power distribution architecture applications.

APPENDIX A

DERIVATIONS

Derivations referenced in the thesis are included in this appendix rather than in the main body for the sake of space and presentation.

A.1 CONSTANT DUTY CYCLE POLAR COORDINATE DERIVATION

From (2.3), (2.5), and (2.6), $\frac{dr}{dt}$ and $\frac{d\theta}{dt}$ need to be derived in terms of r and θ. First, $\frac{dr^2}{dt}$ will be derived and used to determine $\frac{dr}{dt}$ using the identity $\frac{dr}{dt} = \frac{1}{2r}\frac{dr^2}{dt}$.

$$\frac{d}{dt}r^2 = C\widetilde{v_C}\frac{d\widetilde{v_C}}{dt} + L\widetilde{i_L}\frac{d\widetilde{i_L}}{dt} = \widetilde{v_C}\widetilde{i_L} + \overline{i_L}\left(\frac{\widetilde{v_C}^2}{\widetilde{v_C} + \overline{v_C}}\right) - \widetilde{i_L}\widetilde{v_C} = \frac{\overline{i_L}\widetilde{v_C}^2}{\widetilde{v_C} + \overline{v_C}} \tag{A.1}$$

$$\Rightarrow \frac{d}{dt}r^2 = \frac{2\overline{i_L}r^2\cos^2\theta}{C\left(\sqrt{\frac{2}{C}}r\cos\theta + \overline{v_C}\right)} \tag{A.2}$$

$$\Rightarrow \frac{dr}{dt} = \frac{1}{2r}\frac{dr^2}{dt} = \frac{\overline{i_L}r\cos^2\theta}{C\left(\sqrt{\frac{2}{C}}r\cos\theta + \overline{v_C}\right)} \tag{A.3}$$

To derive $\frac{d\theta}{dt}$ in terms of r and θ, the derivative of θ is taken from (2.5), and then the identities in (2.6) are used to simplify.

$$\frac{d\theta}{dt} = \frac{d}{dt}\left(\tan^{-1}\left(\sqrt{\frac{L}{C}}\left(\frac{\widetilde{i_L}}{\widetilde{v_C}}\right)\right)\right) = \underbrace{\left(\frac{1}{1 + \left(\frac{L}{C}\right)\left(\frac{\widetilde{i_L}}{\widetilde{v_C}}\right)^2}\right)}_{A}\underbrace{\left(\sqrt{\frac{L}{C}}\left(\frac{\widetilde{v_C}\dot{\widetilde{i_L}} - \widetilde{i_L}\dot{\widetilde{v_C}}}{\widetilde{v_C}^2}\right)\right)}_{B} \tag{A.4}$$

To aid in comprehensibility, the simplification of expression A and expression B from (A.4) using the identities will be shown separately.

$$A = \frac{1}{1 + \left(\frac{L}{C}\right)\left(\frac{\widetilde{i_L}}{\widetilde{v_C}}\right)^2} = \frac{\frac{1}{2}C\widetilde{v_C}^2}{\frac{1}{2}\left(C\widetilde{v_C}^2 + L\widetilde{i_L}^2\right)} = \frac{r^2\cos^2(\theta)}{r^2} = \cos^2(\theta) \tag{A.5}$$

$$B = \sqrt{\frac{L}{C}}\left(\frac{\widetilde{v_C}\dot{\widetilde{i_L}} - \widetilde{i_L}\dot{\widetilde{v_C}}}{\widetilde{v_C}^2}\right) = \sqrt{\frac{L}{C}}\left(\frac{-\frac{\widetilde{v_C}^2}{L} - \frac{\widetilde{i_L}^2}{C} - \overline{i_L}\left(\frac{\widetilde{i_L}\widetilde{v_C}}{C(\widetilde{v_C}+\overline{v_C})}\right)}{\widetilde{v_C}^2}\right) \tag{A.6}$$

$$= \sqrt{\frac{L}{C}}\left(\frac{-(C\widetilde{v_C}^2 + L\widetilde{i_L}^2) - \overline{i_L}\left(\frac{Li_L\widetilde{v_C}}{(\widetilde{v_C}+\overline{v_C})}\right)}{LC\widetilde{v_C}^2}\right) \tag{A.7}$$

$$= \sqrt{\frac{L}{C}}\left(\frac{-2r^2 - \overline{i_L}\sqrt{\frac{L}{C}}\left(\frac{2r^2\sin\theta\cos\theta}{\sqrt{\frac{2}{C}}r\cos\theta+\overline{v_C}}\right)}{2Lr^2\cos^2\theta}\right) \tag{A.8}$$

$$= \frac{1}{\cos^2\theta}\left(-\frac{1}{\sqrt{LC}} - \frac{\overline{i_L}\sin\theta\cos\theta}{C\left(\sqrt{\frac{2}{C}}r\cos\theta + \overline{v_C}\right)}\right) \tag{A.9}$$

Combining the simplifications of expression A and expression B, $\frac{d\theta}{dt}$ can be obtained.

$$\frac{d\theta}{dt} = AB = \frac{-1}{\sqrt{LC}} - \frac{\overline{i_L}\sin\theta\cos\theta}{C\left(\sqrt{\frac{2}{C}}r\cos\theta + \overline{v_C}\right)} \tag{A.10}$$

A.2 CONTROLLED DUTY CYCLE POLAR COORDINATE DERIVATION

As in Section A.1, $\frac{dr^2}{dt}$ will be derived first and used to determine $\frac{dr}{dt}$ using the identity $\frac{dr}{dt} = \frac{1}{2r}\frac{dr^2}{dt}$.

$$\frac{d}{dt}r^2 = C\widetilde{v_C}\frac{d\widetilde{v_C}}{dt} + L\widetilde{i_L}\frac{d\widetilde{i_L}}{dt} = \frac{\overline{i_L}\widetilde{v_C}^2}{\widetilde{v_C}+\overline{v_C}} + \widetilde{i_L}\left(dE - \overline{v_C}\right) \tag{A.11}$$

$$\Rightarrow \frac{d}{dt}r^2 = \frac{2\overline{i_L}r^2\cos^2\theta}{C\left(\sqrt{\frac{2}{C}}r\cos\theta + \overline{v_C}\right)} + \sqrt{\frac{2}{L}}\left(r\sin(\theta)\right)\left(dE - \overline{v_C}\right) \tag{A.12}$$

$$\Rightarrow \frac{dr}{dt} = \frac{1}{2r}\frac{dr^2}{dt} = \frac{\overline{i_L}r\cos^2\theta}{C\left(\sqrt{\frac{2}{C}}r\cos\theta + \overline{v_C}\right)} + \frac{\sin\theta\left(dE - \overline{v_C}\right)}{\sqrt{2L}} \tag{A.13}$$

$\frac{d\theta}{dt}$ will be derived next, using the identity $A = \cos^2\theta$ shown in equation (A.5) from the start to shorten the derivation.

$$\frac{d\theta}{dt} = \cos^2\theta\left(\sqrt{\frac{L}{C}}\left(\frac{\widetilde{v_C}\dot{\widetilde{i_L}} - \widetilde{i_L}\dot{\widetilde{v_C}}}{\widetilde{v_C}^2}\right)\right) \tag{A.14}$$

$$= \sqrt{\frac{L}{C}}\left(\frac{\cos^2\theta}{\frac{2}{C}r^2\cos^2\theta}\right)\left(-\frac{1}{L}\widetilde{v_C}^2 + \frac{1}{L}\widetilde{v_C}\left(dE - \overline{v_C}\right) - \frac{1}{C}\widetilde{i_L}^2 - \frac{1}{C}\left(\frac{\overline{i_L}\widetilde{i_L}\widetilde{v_C}}{\widetilde{v_C} + \overline{v_C}}\right)\right) \tag{A.15}$$

$$= \left(\frac{\sqrt{LC}}{2r^2}\right)\left(-\frac{C\widetilde{v_C}^2 + L\widetilde{i_L}^2}{LC} + \frac{\widetilde{v_C}\left(dE - \overline{v_C}\right)}{L} - \overline{i_L}\left(\frac{\widetilde{i_L}\widetilde{v_C}}{C\left(\widetilde{v_C} + \overline{v_C}\right)}\right)\right) \tag{A.16}$$

$$= -\frac{1}{\sqrt{LC}} + \frac{\left(dE - \overline{v_C}\right)\cos\theta}{\sqrt{2L}r} - \overline{i_L}\left(\frac{\sin\theta\cos\theta}{C\left(\sqrt{\frac{2}{C}}r\cos\theta + \overline{v_C}\right)}\right) \tag{A.17}$$

Using 2.11 and 2.12 to further substitute, $\frac{d\theta}{dt}$ can be found in terms of only r and θ.

$$\frac{d\theta}{dt} = -\frac{1}{\sqrt{LC}} + \frac{\left(dE - \overline{v_C}\right)\cos\theta}{\sqrt{2L}r} - \overline{i_L}\left(\frac{\sin\theta\cos\theta}{C\left(\sqrt{\frac{2}{C}}r\cos\theta + \overline{v_C}\right)}\right) \tag{A.18}$$

A.3 LOAD CURVE POLAR COORDINATE DERIVATION

In Section 3.2, it is claimed that the constant power line $i_L = \frac{P_L}{v_C}$ in polar coordinates is equivalent to the set of points defined by r_1 and r_2 in (3.6). That proof is presented here in (A.19) - (A.22).

$$i_L = \frac{P_L}{v_C} \quad \Rightarrow \quad \frac{P_L}{r\sqrt{\frac{2}{C}}\cos\theta + \overline{v_C}} = r\sqrt{\frac{2}{L}}\sin\theta + \overline{i_L} \tag{A.19}$$

$$\Rightarrow \quad r^2\frac{2}{\sqrt{LC}}\sin\theta\cos\theta + r\left(\overline{v_C}\sqrt{\frac{2}{L}}\sin\theta + \overline{i_L}\sqrt{\frac{2}{C}}\cos\theta\right) = 0 \tag{A.20}$$

$$\Rightarrow \quad r\left(r + \frac{\overline{v_C}\sqrt{\frac{C}{2}}}{\cos\theta} + \frac{\overline{i_L}\sqrt{\frac{L}{2}}}{\sin\theta}\right) = 0 \tag{A.21}$$

$$\Rightarrow \quad r_1 = 0;\ r_2 = \frac{-\overline{v_C}\sqrt{\frac{C}{2}}}{\cos\theta} + \frac{-\overline{i_L}\sqrt{\frac{L}{2}}}{\sin\theta} \tag{A.22}$$

APPENDIX B

MODEL DETAILS

Figures showing computer models used in the thesis for simulation are included in this appendix rather than in the main body for the sake of space.

B.1 BOUNDARY CONTROL MODEL

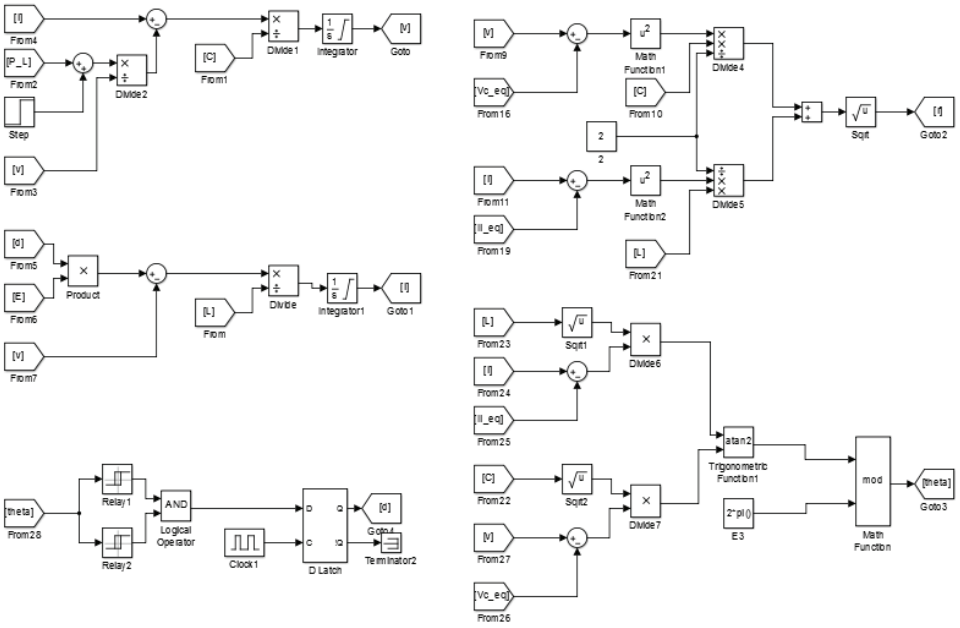


Figure B1: Mathematical Simulink Model of Boundary Controlled Synchronous Buck Converter with CPL

B.2 PD CONTROL MODEL

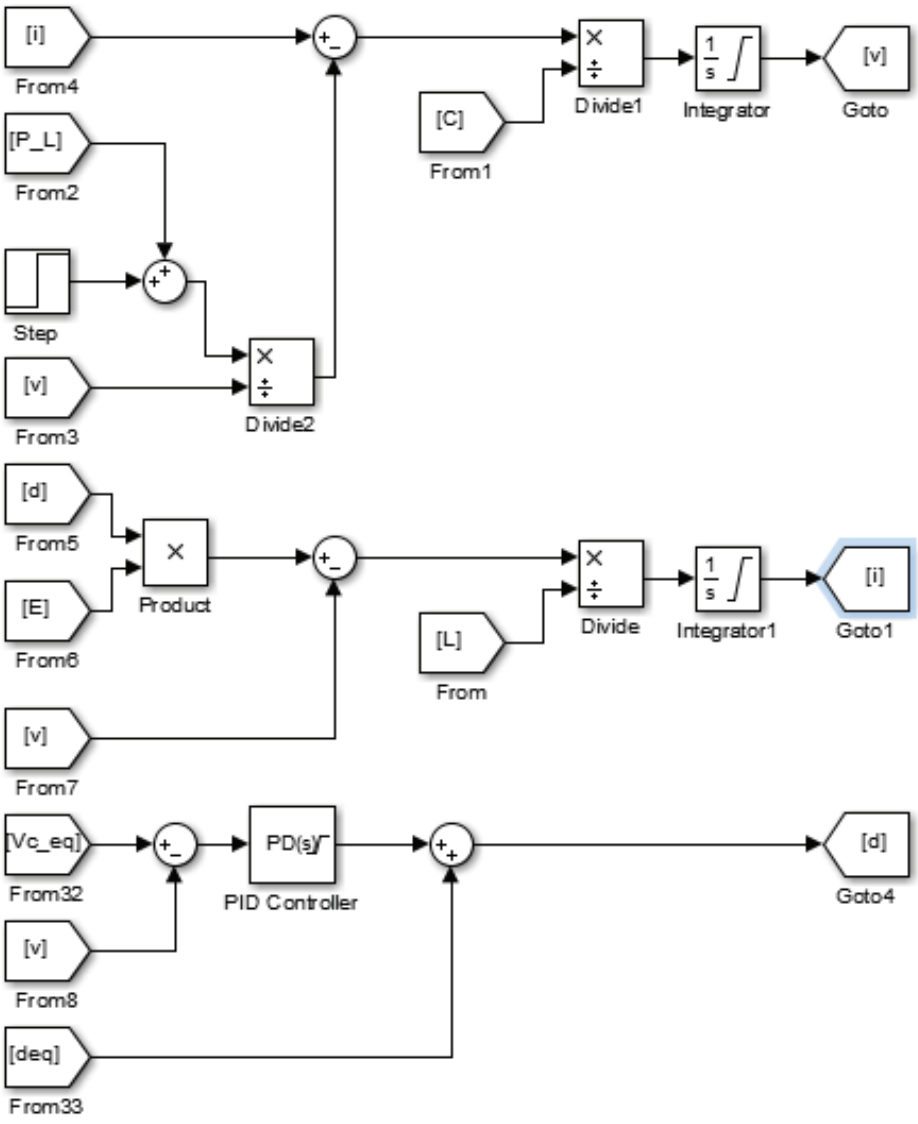


Figure B2: Mathematical Simulink Model of PD Controlled Synchronous Buck Converter with CPL

B.3 PID CONTROL MODEL WITH DISTURBANCES

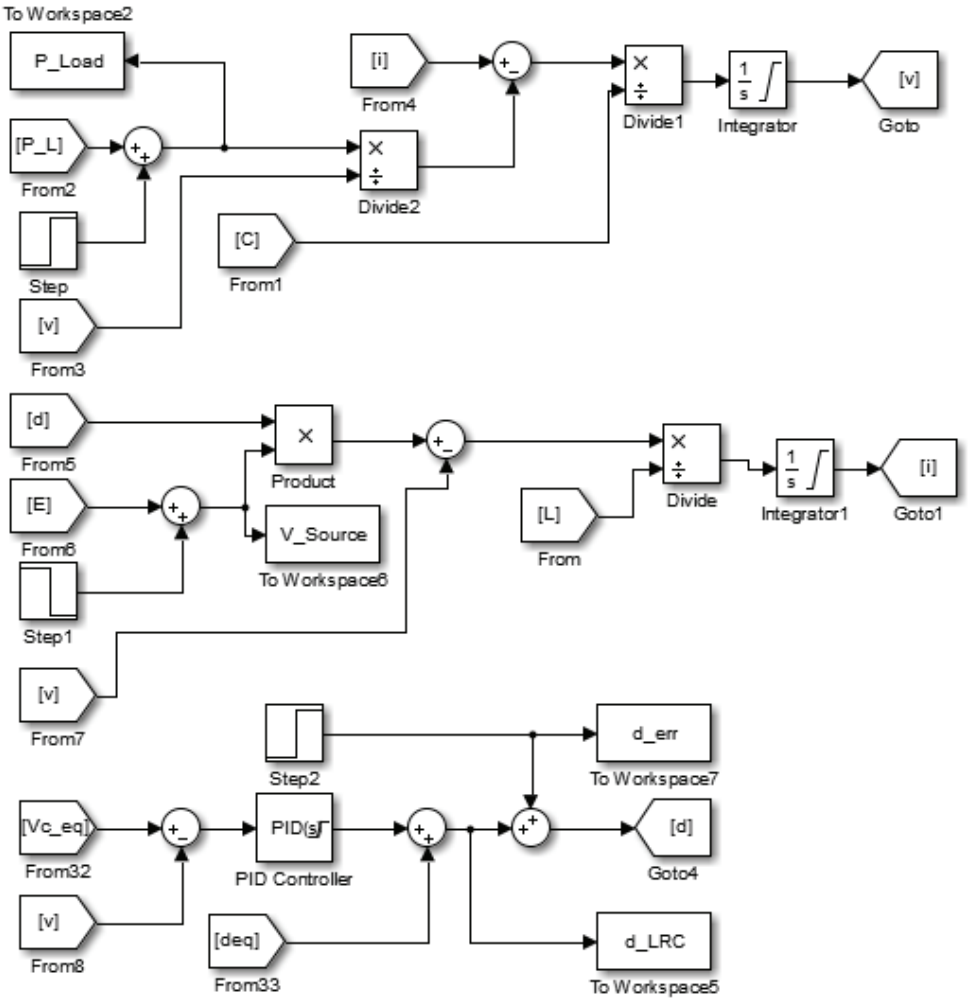


Figure B3: Mathematical Simulink Model of PID Controlled Synchronous Buck Converter with CPL and Disturbances

B.4 COMPONENT MODEL OF SYSTEM WITH CASCADED LRC AND POL CONVERTERS

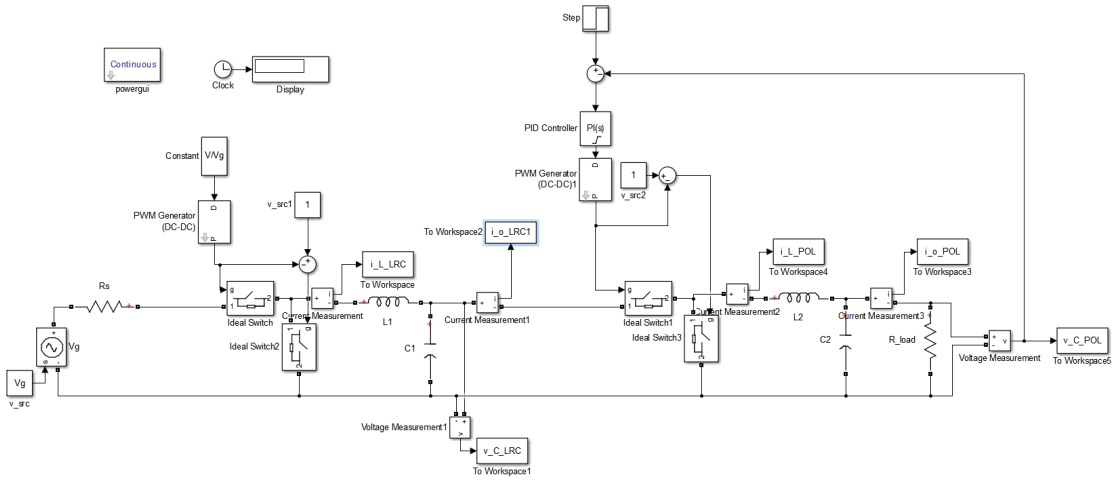


Figure B4: SimPowerSystems Component Model of LRC and POL Converter System

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